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IMPROVEMENT IN GaAs DEVICE YIELD AND PERFORMANCE THROUGH SUBSTRATE DEFECT GETTERING

FINAL TECHNICAL REPORT

BY

T. J. MAGEE

PREPARED FOR:

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
1400 WILSON BOULEVARD
ARLINGTON, VIRGINIA 22209

ATTENTION: DR. RICHARD A. REYNOLDS

MONITORED BY:

OFFICE OF NAVAL RESEARCH
DEPARTMENT OF THE NAVY
800 NORTH QUINCY STREET
ARLINGTON, VIRIGINIA 22217

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(10) T. J. Magee, J. Peng, R. Ormond, R. A. Armistead, M. Malbon, and C. A. Evans, Jr.†

Avantek, Inc., †C. Evans and Associates

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The use of mechanically-produced, back-surface damage as a means of gettering impurities and defects in GaAs wafers has been investigated. Comparative analyses have been done on both ion implantation and mechanical back-surface-damage-gettering techniques. The increased thermal stability of mechanically-produced damage has shown ion-implantation techniques to be less effective for gettering over long anneal periods at elevated temperatures. Stress gradients produced by graded dislocation distributions produce reductions in front-surface defect concentrations and effective gettering of Au and Cr at

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the back surfaces. Thermal stability times of back-surface damage at anneal temperatures of 700-800°C is typically on the order of 2 - 3 hours, corresponding to the point at which major back-surface microstructural damage is largely annealed. Increases in the thermal stability period were attained by encapsulating the back surface with an As-doped SiO_2 layer.

Gettering of Cr by back-surface damage was also investigated at low temperatures (300°C - 400°C) for anneal periods of 10 - 300 hrs. Measurable concentrations of Cr were detected with the process characterized by an activation energy of $\sim$ 0.88 eV and a time-dependent term, exp ($\theta t^{\frac{1}{2}}$).

Using the developed gettering procedures, FET structures were fabricated on VPE layers on pre-gettered GaAs wafers. Dramatic improvements in yield per wafer, noise figures at higher frequences and input capacitance values were obtained on "inscreened" wafers processed through a normal fabrication line.

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1. INTRODUCTION

1.1 BACKGROUND

The influence of surface damage and secondary or included growth defects on the electrical transport properties of elemental and compound semiconductors has been well established and documented in articles and technical reports published over the past decade. A number of investigators have used defects introduced at a surface by mechanical means,[1-4] or by ion implantation[5-8] to control defect or impurity gettering from the opposite surface of the semiconductor. The largest number of studies has been directed toward improving the quality and ultimate device yield of silicon wafers. However, recent applications of back-surface-damage-gettering techniques to GaAs wafers have shown considerable promise for improving the quality of GaAs-based FETs.

Studies at the IBM Fishkill Laboratory by Schwuttke and Yang[1] have demonstrated that back-surface mechanical damaging of GaAs wafers by impact sound stressing can effectively reduce the front-surface concentration of defects and the number of dislocation lines propagating from the wafer into active epitaxial layers grown on the surface of the material. However, there have been no detailed studies to optimize back-surface-damage techniques and extend this application to actual fabrication of device structures. In addition, no detailed information has been published on the effectiveness of controlled damage in impurity gettering GaAs. It is of particular interest to determine whether gettering of impurities such as chromium and other heavy metals can be obtained, since these are known to be responsible in part for the "mobility/concentration dip" effect in epi-layers grown on GaAs substrates. The relative efficiencies of back-surface gettering of defects and impurities by either mechanical damage or ion-implantation-produced damage has also not been previously established.

The objective of this study was to investigate and compare back-surface-damage techniques in regard to defect and impurity gettering in an attempt to optimize procedures that would be adaptable for production-line processing of devices. The first phase of this program was directed toward a detailed investigation of gettering procedures, while the second phase was concerned with both the production/testing of device structures on GaAs and more extensive investigations of Cr gettering in GaAs. This report presents a summary of data obtained on this program.

1.2 SUMMARY OF RESULTS

Research conducted on this program has resulted in the development of back-surface gettering procedures that have been shown to be effective in improving the performance and yield of devices fabricated either within epitaxial layers or directly on GaAs substrates. In addition, the first observation of the motion, gettering and redistribution of Cr in GaAs was initially reported on this program in 1978. Simultaneous research at Plessey Labs in England during this period provided additional confirmation of the redistribution of Cr in GaAs. Since this time, a number of laboratories have conducted studies on Cr motion that have had a significant impact on GaAs material processing.

For this program, the following results have been obtained:

- Identification of gettering induced by dislocation line distributions as a function of abrasive particle size, rotation rate, and exposure time of the wafer.

- Identification of front-surface-defect-gettering efficiencies for variable back-surface-defect concentrations.

- Consistent evaluation of Cr and Au defect gettering by dislocation structure at the back surface.

- Investigation of defect stability times or maximum allowable processing times at 800°C for effective gettering.

- Identification of encapsulation layer gettering effects and the correlation of these effects with Ga and As outdiffusion.

- Comparison of mechanical and ion-implantation gettering of defects at the front-surface.

- Identification of impurity "reverse" annealing or de-gettering effects.

- Analysis and identification of Cr gettering and reverse annealing effects by back-surface-damage regions.

- Improvement in back-surface-damage stability times using an As-doped SiO_2 encapsulation layer on the back of the wafer.

- Identification of Cr gettering and outdiffusion during alloying (350°C) of contact structures on GaAs.

- Growth of low-defect-concentration VPE layers on back-surface (pre-gettered) Cr-doped substrates.

- Reduction of Cr outdiffusion into VPE layers grown on pre-gettered Cr-doped substrates.

- o Improved electrical properties of VPE layers on Cr-doped substrates.

- o Improvement in the electrical parameters and the device yield of FET structures fabricated in VPE layers on pre-gettered (Cr-doped) substrates.

- o Identification of low-temperature ($\leq 350^{o}C$) Cr-gettering in GaAs.

- o Identification of B concentrations in LEC and Bridgman-grown GaAs.

- o Investigation of damage annealing and Cr redistribution in B-implanted GaAs samples.

1.3 PUBLCATIONS

The following publications were drawn in part or in total from this program of research:

a) "Back-Surface Gettering and Cr Out-Diffusion in VPE GaAs Layers," Appl. Phys. Lett. 35, 277 (1979).

b) "Alloying of Au Layers and Redistribution of Cr in GaAs," Appl. Phys. Lett. 35, 615 (1979).

c) "Getering of Au by Back-Surface Damage in GaAs," Phys. Stat. Sol. (A) 55, 161 (1979).

d) "Back-Surface Gettering of Cr in GaAs," Phys. Stat. Sol. (A) 55, 169 (1979).

e) "Outdiffusion of Cr in VPE GaAs Layers and Back-Surface Gettering," Extended Abstracts, Vol. 79-2, ECS Meeting, Los Angeles, CA, October 14-19, 1979.

f) "Incorporation of Boron During the Growth of GaAs Single-Crystals," Appl. Phys. Lett. 36, 989 (1980).

g) "Low-Temperature Gettering of Cr in GaAs", Appl. Phys. Lett. 37, 53 (1980).

h) "Low-Temperature Redistribution of Cr in Boron-Implanted GaAs in the Absence of Encapsulant Stress," submitted for publication, (Appl. Phys. Lett., 1980).

i) "Annealing of Damage and Redistribution of Cr in Boron-Implanted, Si_3N_4-Capped GaAs," submitted for publication (Appl. Phys. Lett., 1980).

2. EXPERIMENTAL PROCEDURE AND APPARATUS

The laboratory apparatus for mechanically creating controlled back-surface damage in small samples is shown schematically in Figure 1. The teflon base of the unit is supported by rods that are connected to lab stands and a clear lucite cylindrical cover fitted into a circular groove notched into the base plate. A spring-loaded metallic sample stand is used to provide vertical pressures up to 150 psi against the rotating abrasive disk. Abrasive cloth attached to the disk is used to produce mechanical damage during operation. Since alignment of the rotating disk with respect to the sample is extremely critical for uniform damage production at the back surface, the support fixture for the drive shaft connecting the motor and rotating disk was designed so that critical vertical and horizontal adjustments could be made before any experimental run. Rotary motion of the disk is provided by an external motor connected to the vertical head by a flexible drive shaft. Angular velocity is controlled by varying the input to the motor with a maximum rotation rate of 25,000 rpm recorded in the free running state, and 22,000 rpm in a typical run mode. In all cases, it was necessary to determine the rotation rate as a function of vertical pressure of the sample against the rotating disk. Total exposure time is monitored and control provided manually or automatically for pre-set time intervals.

Samples are mounted on the smooth face of the sample stand and the force adjusted by altering the compression of the spring attached to the stand. During operation of the unit, it was found that the flow rate of deionized water must be controlled carefully to provide proper cooling of the sample and removal of mass during abrasion. Total exposure or operational time was also extremely critical for GaAs wafers, although relatively less so for damage introduction in Si. In each case, the time of exposure was monitored and controlled manually or with an automatic "on-off" electronic timer.

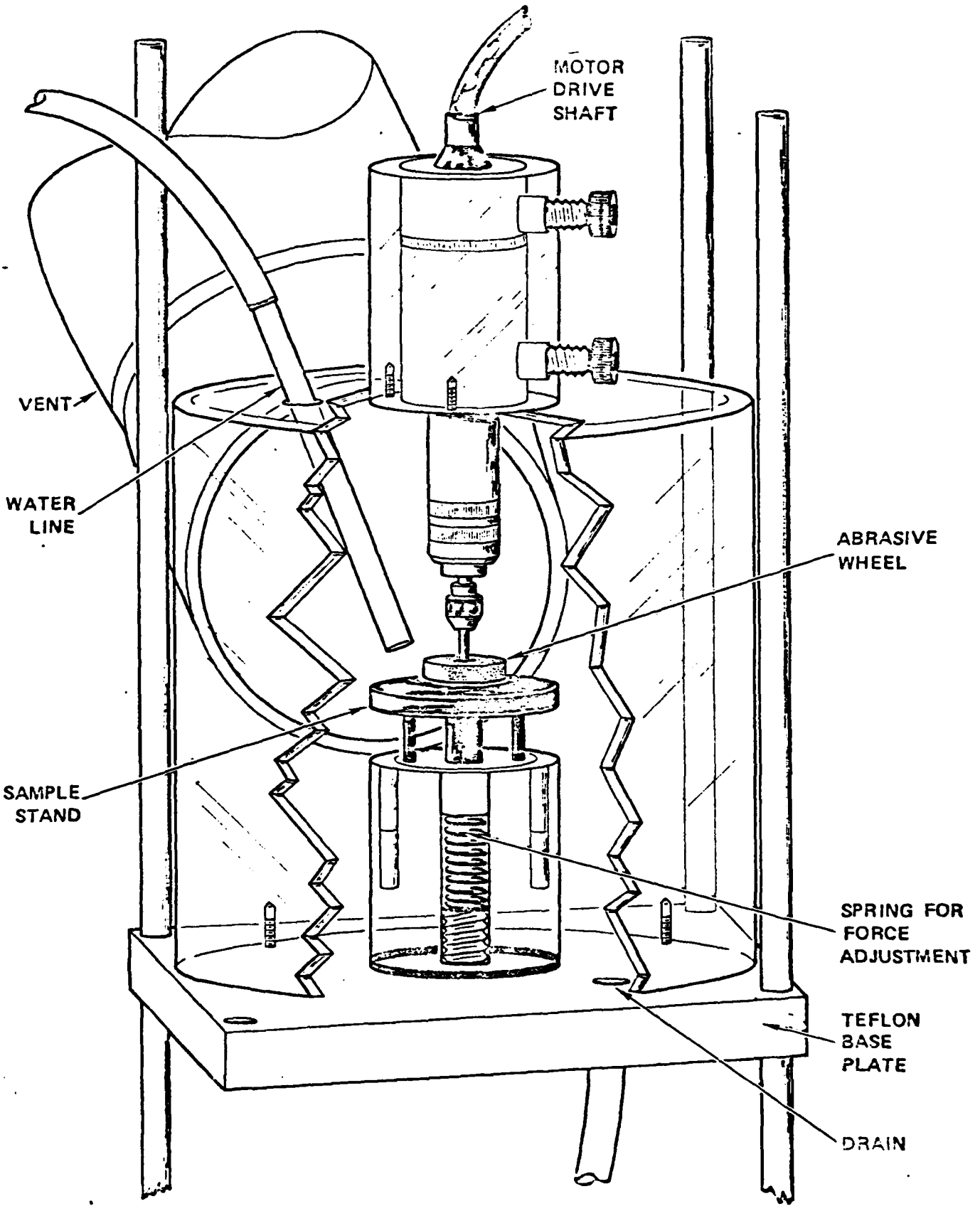


FIGURE 1. EXPERIMENTAL APPARATUS FOR CREATING BACK-SURFACE MECHANICAL DAMAGE

3. DAMAGE DISTRIBUTION AND STABILITY

3.1 MICROSTRUCTURAL DAMAGE

Gallium arsenide wafers used in this experiments were obtained from Crystal Specialties, Inc., Monsanto, and Laser Diodes. The samples were of (100) orientation ($\pm$ 1^{o}) and doped with Cr or Si to levels of 0.008 and 10^{8} Ωcm, respectively. Specimens were prepared for back-surface-damage experiments in the form of parallelopipeds of 5 mm x 5 mm lateral dimensions with a thickness of approximately 0.38 - 0.51 mm.

TRI-M-ITE (3M Corp.) paper disks containing silicon carbide particles of sizes 0.3 μm, 12.5 μm, 30 μm, and 60 μm, were used in these experiments. Rotation rates were varied between 1000 to 10,000 rpm and the sample exposure time was systematically altered in the range, 30 sec to 180 sec. A stationary platform pressure of 47 psi was experimentally found to yield the most adequate and reproducible results.

Samples for transmission electron microscopy/diffraction (TEM/TED) analysis were prepared by conventional jet thinning from 2.5 mm x 2.5 mm specimens. To establish control data for each of the experiments, the microstructure of samples cut from as-received wafers was analyzed at both the front and back sides of polished specimens.

Figure 2 shows a representative series of bright-field electron micrographs obtained from GaAs wafers damaged at the back surface using a 30 μm abrasive particle size, 8,000-rpm rotation rate and exposure times between 30 sec and 3 min. At a 30-sec exposure time, edge dislocations lying in the (100) plane and inclined dislocation lines form continuous forested nests extending beneath the surface. After 1 min and 3 min of exposure, the

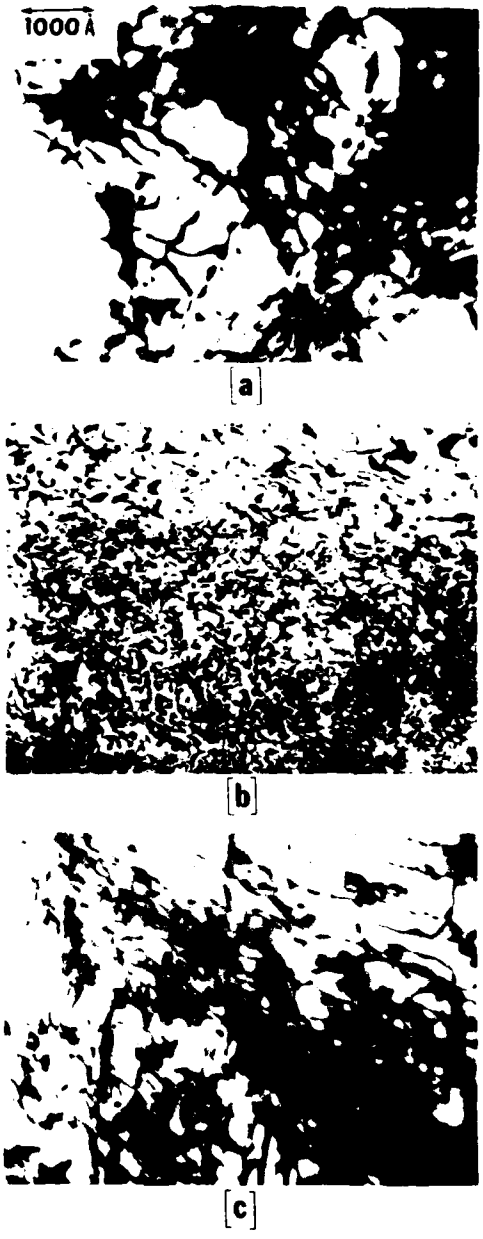


FIGURE 2. BRIGHT-FIELD TRANSMISSION ELECTRON MICROGRAPHS OF BACK-SURFACE-DAMAGED GaAs WAFERS (PARTICLE SIZE = (0.3 μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 7000 Å; c) d = 1.4 μm

dislocation density increases significantly and extremely complex forested regions are formed. The abrasive process produces a region of mass removal and circular grooves extending into the substrate at the back surface.

After 30 sec of exposure $\sim$0.7 mil of back-surface material is removed and grooves extending to a depth of $\sim$1.2 mils are observed in the scanning electron microscope. Similar groove depths are detected after 1 min and 3 min of exposure, but the mass removal thickness increases to $\sim$2.0 mils and 5 mils, respectively. Experiments conducted at similar exposure times using particle sizes of 0.3 μm, 12.5 μm and 60 μm, show that the amount of mass removed increases significantly after 3 min of exposure and groove heights are approximately equal to the particle size.

In contrast to results obtained on Si, where broader, more complex grooving occurs as a function of exposure time, the distribution of grooving is relatively independent of exposure time. However the mass removal rate is greatly increased for GaAs, and short exposure times are desirable. The results of experiments conducted under similar conditions, with the rotation rate varied between 2000 and 8000 rpm, suggested that the most uniform distribution of macroscopic damage was obtained at 8000 rpm.

In sharp contrast to earlier studies and to practices currently used by manufacturers in back-surface damage of Si wafers, we found that assessments of the concentration of microscopic damage introduced into the GaAs substrate cannot be characterized by the depth or distribution of macroscopic grooves and/or pits produced at the back surface. TEM analysis must be used routinely in these appplications to identify the distribution of microstructural defects. In Figures 3 through 6, transmission electron micrographs show the distribution of damage at various depths for samples subjected to rotary abrasion at 8000 rpm for 30 sec at a vertical stage pressure of 47 psi, using particle sizes of 0.3 μm,

FIGURE 3. BRIGHT FIELD TRANSMISSION ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (0.3 μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 7000 Å; c) d = 1.4 μm.

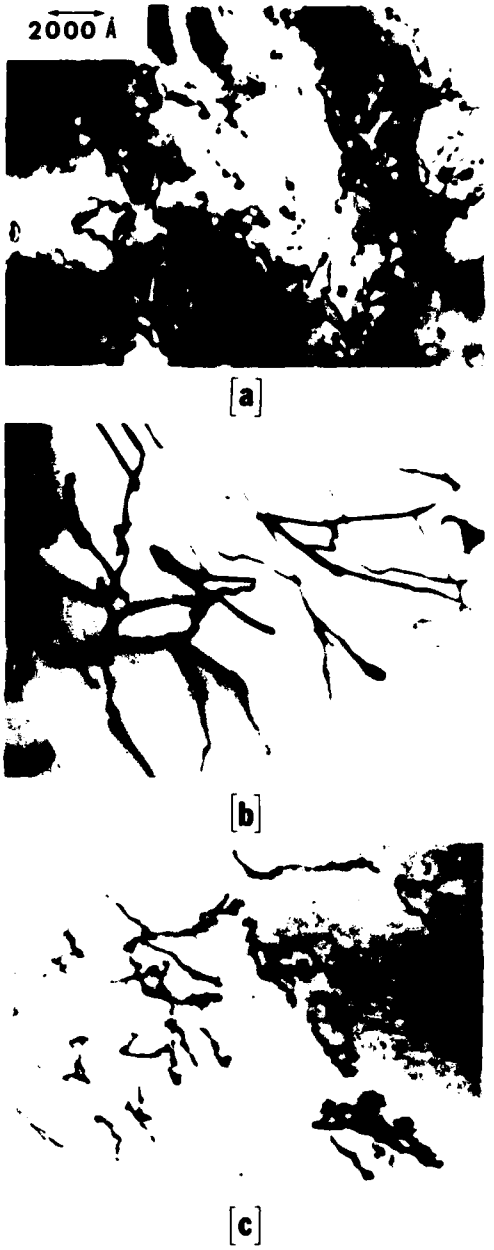


FIGURE 4. BRIGHT-FIELD TRANSMISSION ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (12.5-μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 6000 Å; c) d = 1 μm.

FIGURE 5. BRIGHT-FIELD TRANSMISSION ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (30-μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 4000 Å; c) d = 1 μm.

FIGURE 6. BRIGHT FIELD ELECTRON MICROGRAPHS OF SECTIONED WAFERS SHOWING DAMAGE AT DEPTH (60-μm ABRASIVE PARTICLES); a) d = 1000 Å; b) d = 7500 Å; c) d = 10.2 μm.

12.5 μm, 30 μm and 60 μm, respectively. In all cases, we observed a distribution of microstructural damage extending beneath the region of mass removal and macroscopic grooving. Hence, the experimental conditions used produced a laterally-continuous sheet of dislocation lines in forested arrays and tangles that extend to a maximum observable depth of 1.5 m below the depth of grooves at the back surfaces. In Figures 3 - 6, we observe that the maximum near-surface concentration is produced for the larger particle sizes. In addition, the density of dislocation lines decreases rapidly as a function of depth for the smaller particle sizes. In all samples examined, we detected no dislocation line structure at depths exceeding 1.5 μm.

In Figure 7, we show a plot of the dislocation line length density, $\rho(cm/cm^3)$, at various depths from the back surface for the variable particle sizes used. For a particle size of 0.3 μm, the dislocation line density decreases from 3.7×10^9 cm/cm^3 in the near-surface region to negligibly small concentratons at depths $\sim$ 1.5 μm. As the particle size is increased, the dislocation density also increases to a maximum of 7.2×10^{10} cm/cm^3 (particle size = 60 μm). In each case, we observe a negligible line density at depths $\sim$ 1.5 μm. Of particular interest, however, is the presence of a graded dislocation density observed reproducibly for samples used in these experiments. The slope of the concentration versus-depth line increases rapidly as a function of particle size, approaching saturation for particle sizes $\sim$30 μm.

The data show that the rotary back-surface-damage technique produces a graded defect layer, rather than a uniform layer of constant defect concentration. This result is of significance to the back-surface-gettering procedure, since the resulting strain field at the back surface will also be sharply graded and defect and impurity gettering will be subsequently influenced, as discussed in the next sections.

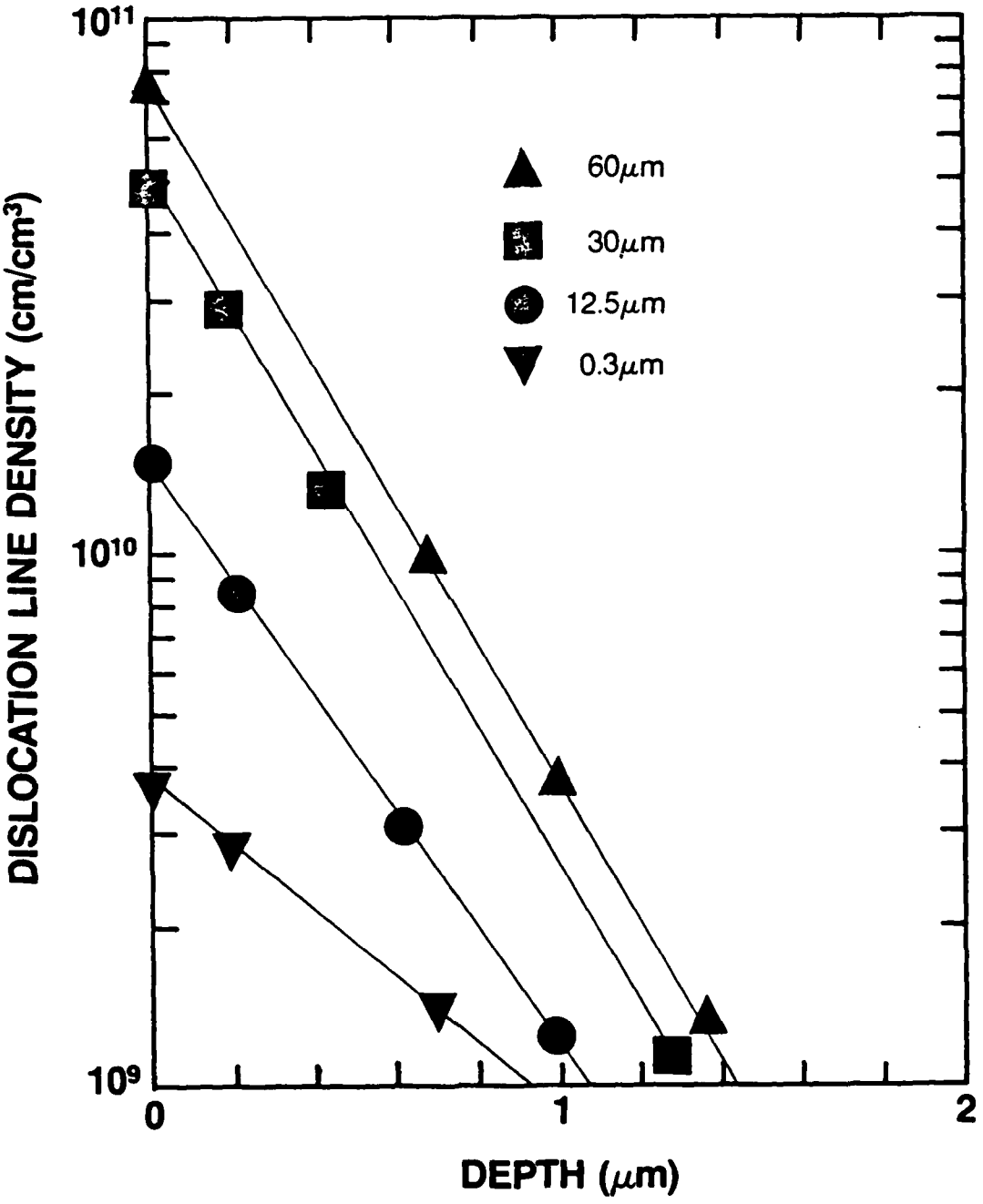


FIGURE 7. DISLOCATION LINE DENSITY VS DEPTH FOR VARIOUS PARTICLE SIZES (8000 rpm, 30 sec).

3.2 THERMAL STABILITY

To evaluate the applicability of the gettering technique to a device processing line, it is necessary to define a stability time or period in which the defects will be retained at temperatures aproaching those normally encountered in routine device fabrication or processing procedures. Therefore, we conducted a series of experiments in which back-surface-damaged wafers were coated on the front surfaces with a low-oxygen-content, plasma-deposited Si_3N_4 layer formed at 300°C and annealed at 800°C for periods in the range, 1/2 hr. to 6 hrs. After annealing, the nitride layers were removed and the samples prepared for TEM analysis by jet thinning from the front surface. Figure 8 shows a representative transmission electron micrograph obtained at the back surface of samples before and after annealing at 800°C for variable periods. As anticipated, we note a reduction in dislocation density as a function of annealing duration. In Figure 9, we show a plot of the unannealed fraction of dislocation lines

$$\left(\frac{\sum_{i=1}^{n} \rho i(x)}{\sum_{i=1}^{n} \rho o(x)} \right)$$

as a function of annealing time at 800°C.

The increased dislocation density and complex forests produced by the larger particle sizes will require longer annealing times, whereas for the smaller particle sizes, annealing will occur more rapidly. In all cases, residual dislocation structures will remain in the samples after extended anneals at 800°C However, for σ = 60 μm,(unannealed damage factions < 10 to 15%), gettering by dislocations will be ineffective. Similarly, residual structure remaining in samples damaged by smaller particles will not be efficient for impurity and defect gettering. Hence, a maximum stability time for gettering by dislocation lines at the back surface

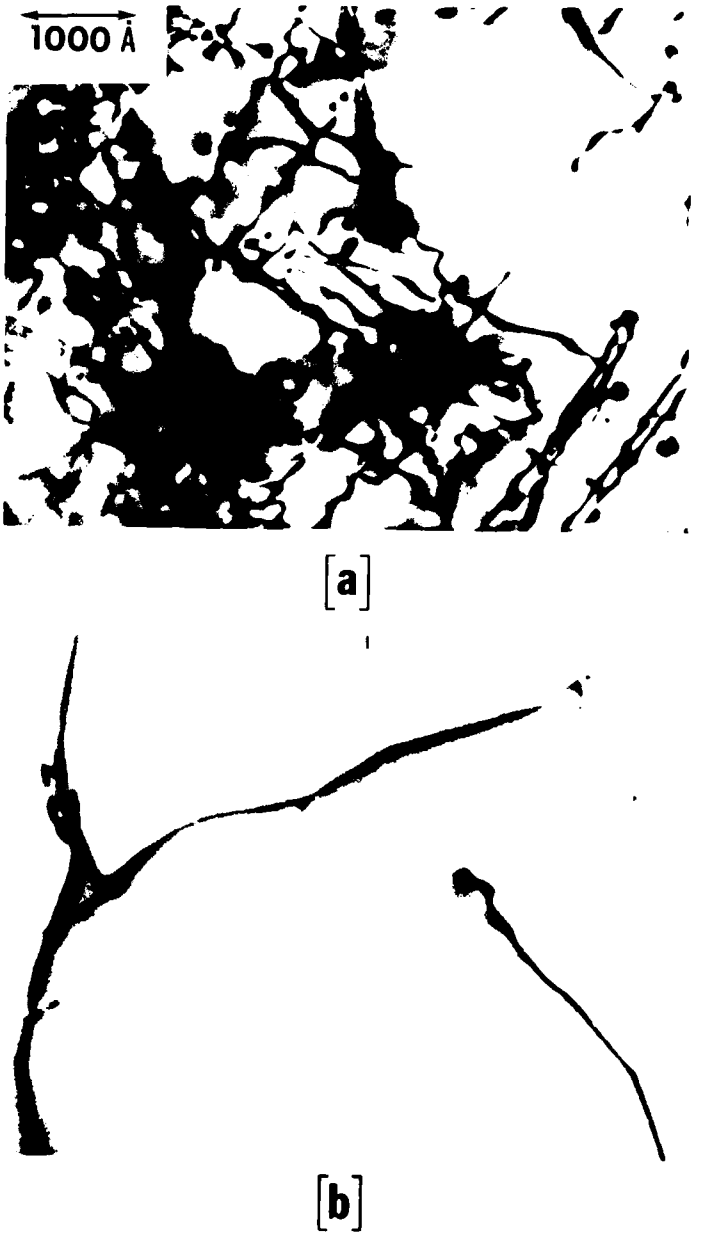


FIGURE 8. BRIGHT-FIELD ELECTRON MICROGRAPHS OF BACK-SURFACE-DAMAGED WAFERS (30 μm PARTICLE SIZE, 8000 rpm, 30 sec) AFTER ANNEALING; a) 30 min; b) 180 min.

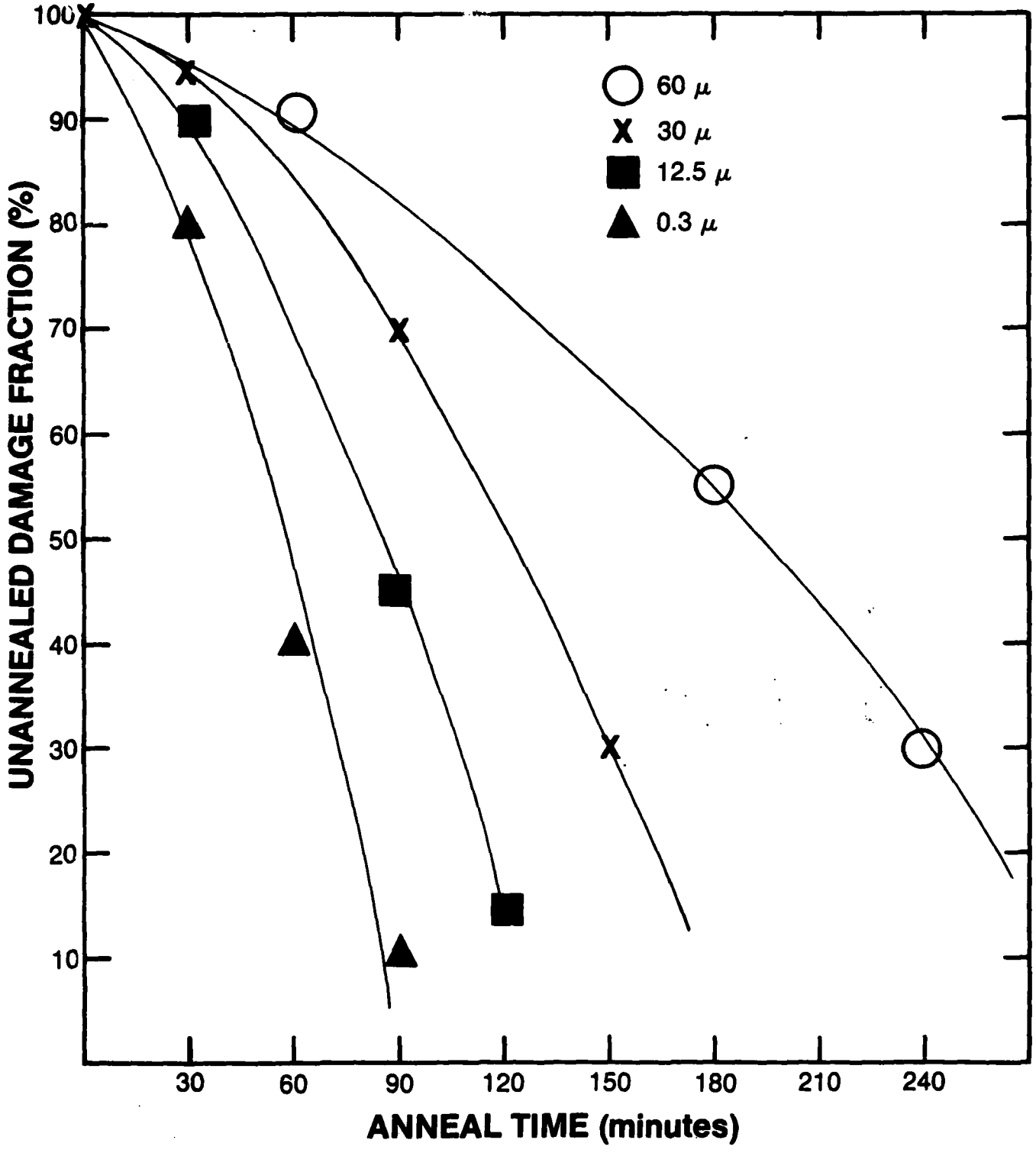


FIGURE 9. UNANNEALED FRACTION OF DAMAGE REMAINING AS A FUNCTION OF ANNEALING TIME.

is between 4 and 5 hrs. If the annealing time exceeds the damage stability time, then "reverse" annealing or "reverse" impurity gettering will likely occur, as has been noted in Si.

4. EFFECTS OF ENCAPSULATION LAYER

Since dielectric layers are routinely used as annealing caps for gettering or ion-implantation studies, it is essential that the encapsulation layers be examined to determine possible gettering or deleterious effects caused by the encapsulant during annealing. In previous studies by the author[9-12] and others,[13,14] it was shown that the presence of oxygen in silicon nitride encapsulating layers is associated with the outdiffusion of Ga and As from the GaAs substrates during annealing.

Alterations at the surface of a GaAs substrate annealed with nitride caps containing oxygen are also noted in the form of brown discoloration zones or layers relatively inert to chemical etching. Bozler, et al,[8] in studies of SiO_2/Si_3N_4 capped ion-implanted (back surface) GaAs samples, reported the presence of an inert surface layer after annealing and a slight or apparent cap-gettering effect on control (undamaged) wafers. In this investigation, we were concerned about possible gettering effects by the encapsulant and whether the currently used plasma deposited caps would be adequate for gettering studies. Silicon nitride caps used in this study were formed by low-temperature ($300^{o}C$) plasma deposition on GaAs at Avantek, Inc. Auger electron spectroscopy (AES), combined with in-situ Ar-ion milling, was used to obtain the chemical/depth profiles of the Si_3N_4 (GaAs) structures. The AES data were obtained by irradiating the sample with a 3-kV, 10-A electron beam and monitoring the differential specturm of secondary electrons with a cylindrical mirrow analyzer during Ar-ion sputtering at a vacuum level of 5×10^{-5} Torr. A standard semiquantitative formalism[15] was used to analyze the AES data.

In Figures 10 and 11, we show representative chemical depth profiles (normalized) obtained on Si_3N_4/GaAs structures before annealing and after a 30-minute anneal at 800°C in a flowing H_2 atmosphere. The unannealed sample shows residual oxygen present throughout the film with no initial Ga or As outdiffusion from the substate. After annealing, the second sample clearly shows that Ga and As have outdiffused from the substrate through the encapsulant to accumulate on the surface of the nitride film. This result is in agreement with recent results that show oxygen content in the nitride can be correlated with outdiffusion of Ga and As.

In separate experiments, we removed the caps of control and annealed structures by immersing them in a dilute HF solution. Examination in an optical microscope and scanning electron microscope (SEM) showed no apparent modification, discoloration or pitting at the surface.

To provide further comparison, we did AES profiling on Si_3N_4 caps known to contain a high concentration of oxygen. In Figure 12, we show the normalized AES profile of the annealed (850°C) Si_3N_4/GaAs structure. It is apparent that Ga has outdiffused through the cap to the surface of the film. However, in comparison to the results shown in Figures 10 and 11, the oxygen concentration is higher and the amount of Ga outdiffusion greater. After annealing, the same cap was removed in a separate experiment and examined optically and in a SEM. In both cases, a slightly discolored or nonuniform surface was observed with small regions showing resistance to conventional chemical etching.

We next prepared two sets of samples from the Si_3N_4 capped wafers provided by Avantek. In the first set of samples, the nitride layers were removed from the substate by immersing the structure in a dilute HF solution. The remaining samples were

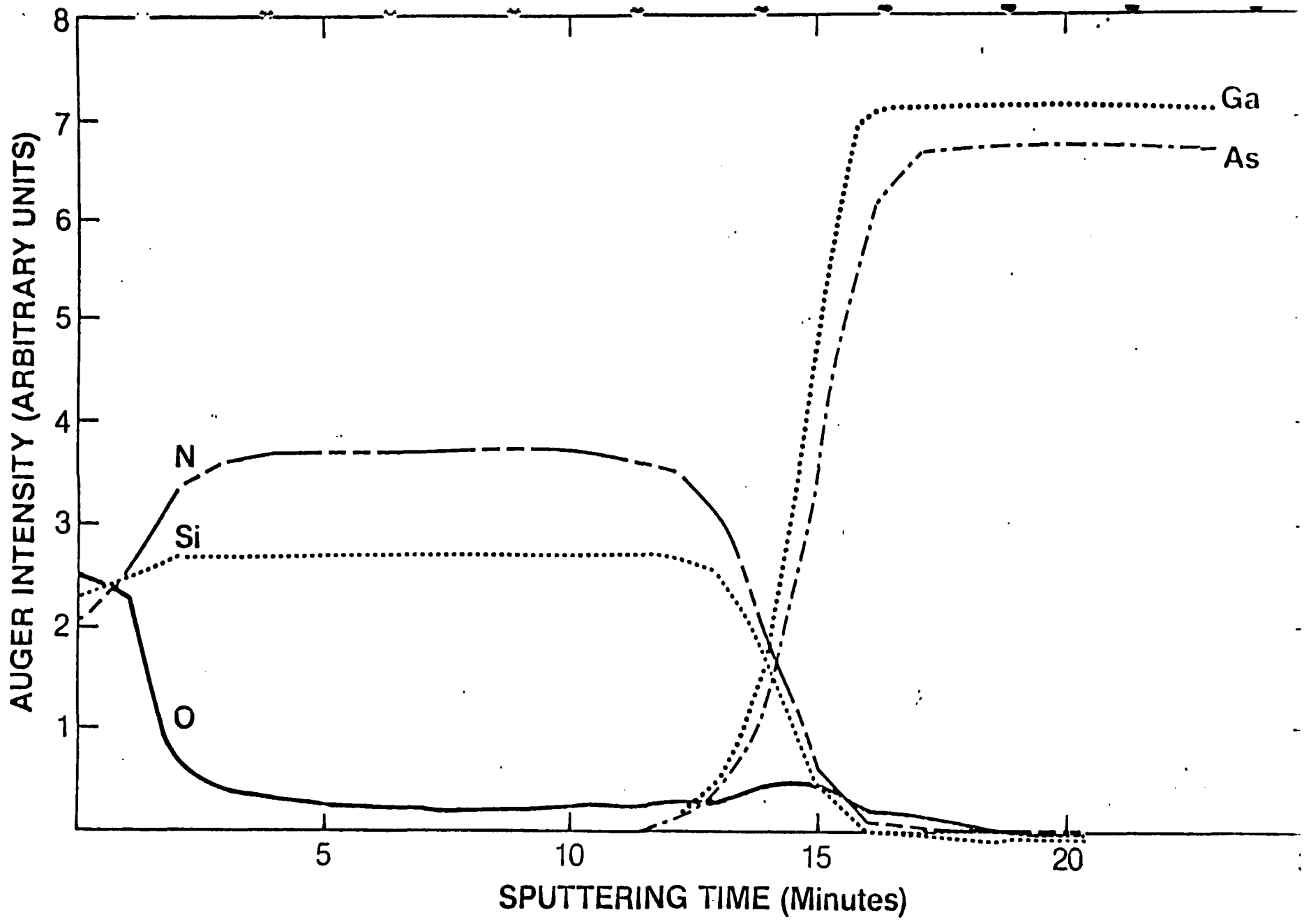


FIGURE 10. AES CHEMICAL DEPTH PROFILE (NORMALIZED) OF AS-DEPOSITED Si_3N_4 FILM ON GaAs.

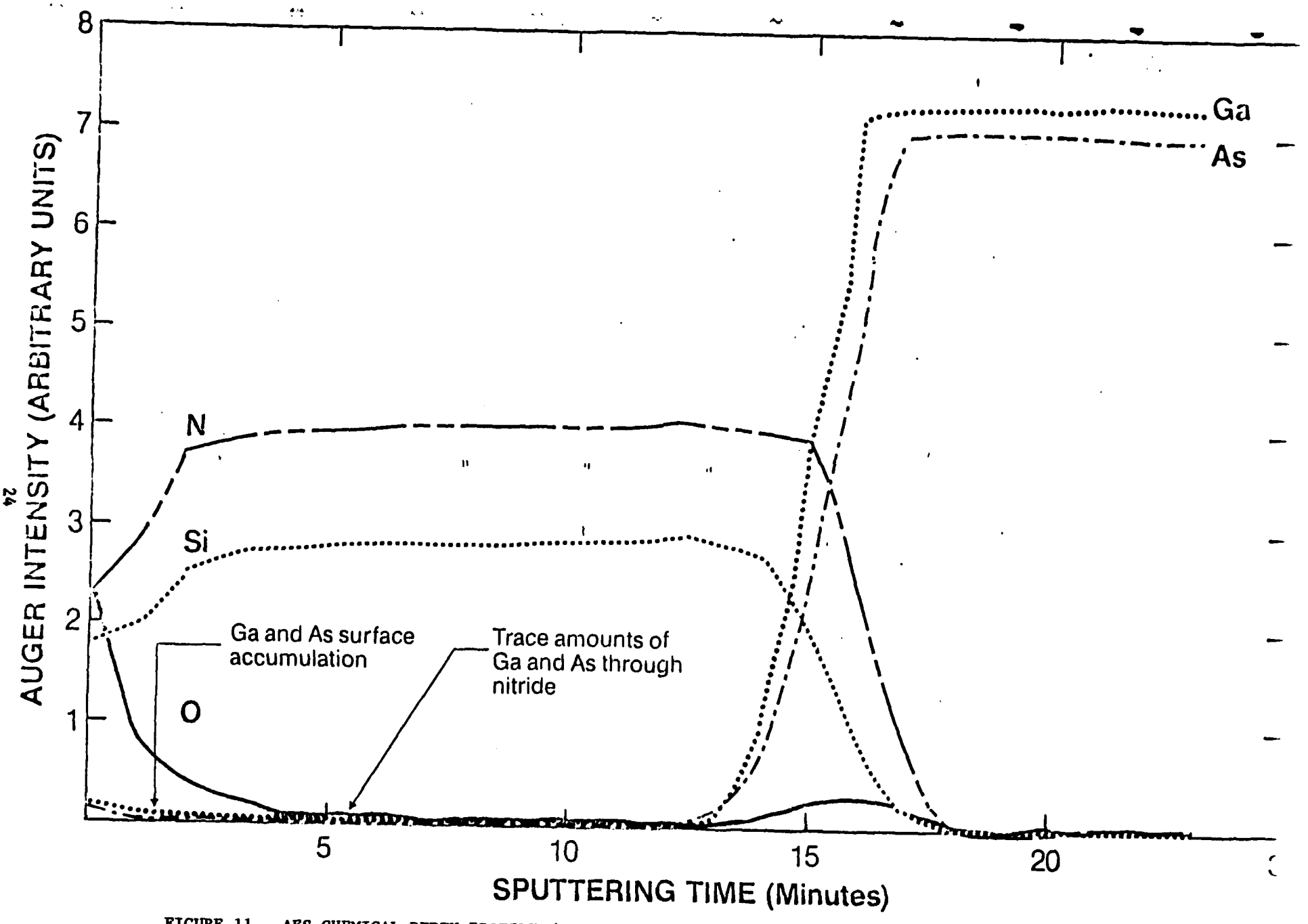


FIGURE 11. AES CHEMICAL DEPTH PROFILE (NORMALIZED) OF Si_3N_4 FILM ON GaAs.

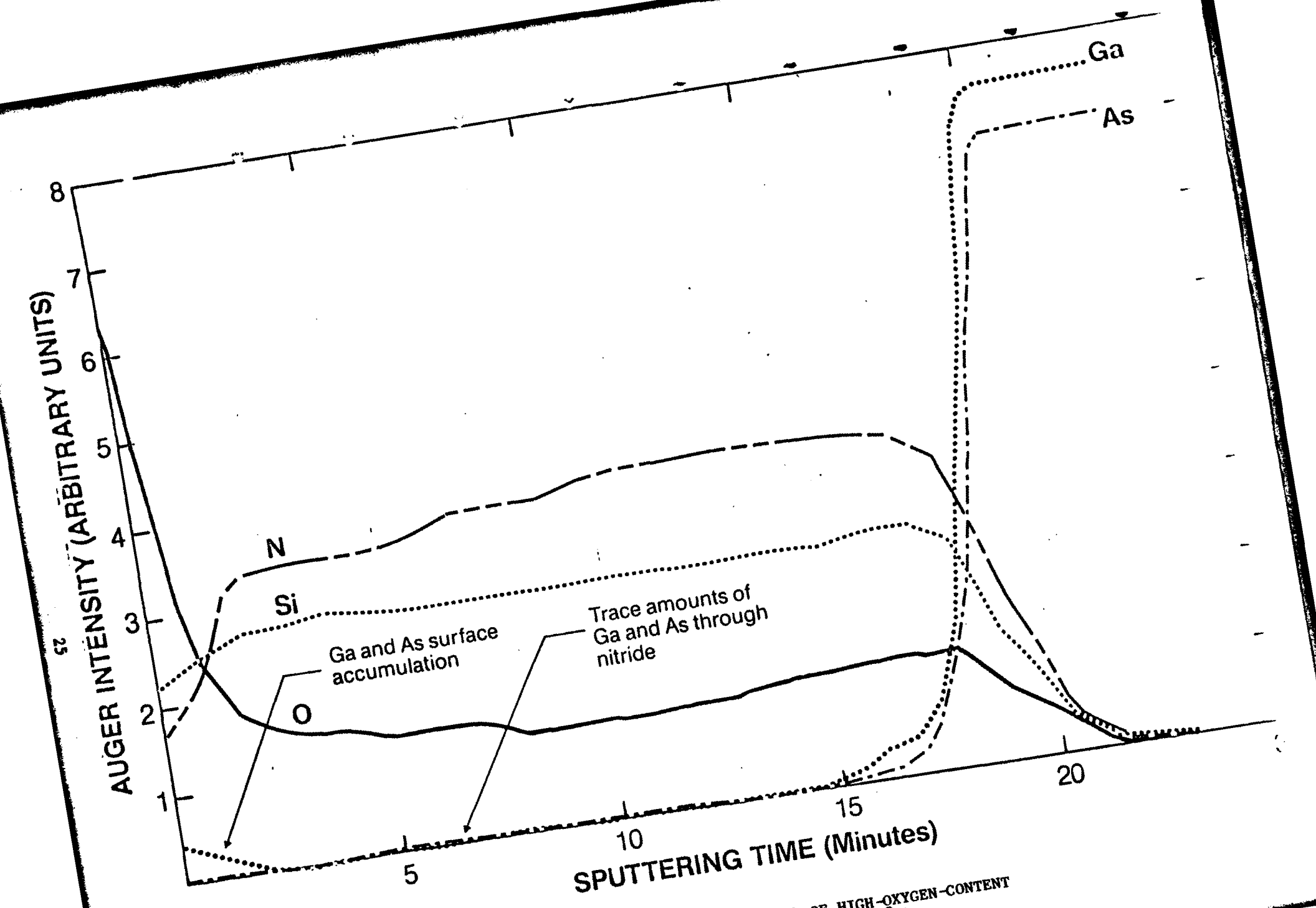


FIGURE 12. AES CHEMICAL DEPTH PROFILE (NORMALIZED) OF HIGH-OXYGEN-CONTENT Si_3N_4 FILM ON GaAs AFTER ANNEALING (30 min., 850°C).

first annealed at 800°C for 30 min in H_2 and the cap subsequently removed in HF. All samples were then immersed in a standard H_2SO_4:H_2O_2:H_2O (3:1:1) solution to expose defects or etch features on the (100) surface. Figure 13 shows representative optical micrographs of control and annealed sample surfaces after etching. Comparing Figure 13a) (control) and Figure 13b) (capped, annealed), we observe a slight reduction in the surface defect density, indicating a small apparent reduction in surface defect concentration. We then repeated the experiments on several sets of samples with essentially identical results, thereby supporting the contention that the encapsulant may exercise a small, but perceptible, defect gettering effect.

From the data obtained, we conclude that the quality of encapsulting layers can exercise some influence on defect gettering at the front surface. It is also apparent that outdiffusion of Ga and As should be suppressed, particularly for long annealing periods. In the present experiments, the oxygen concentration in nitride films can be correlated with Ga and As outdiffusion and the creation of vacancies in the rear surface region. The small gettering effect observed can then be associated with the presence of excess Ga and As vacancies at the surface or differential strain within the interfacial region.

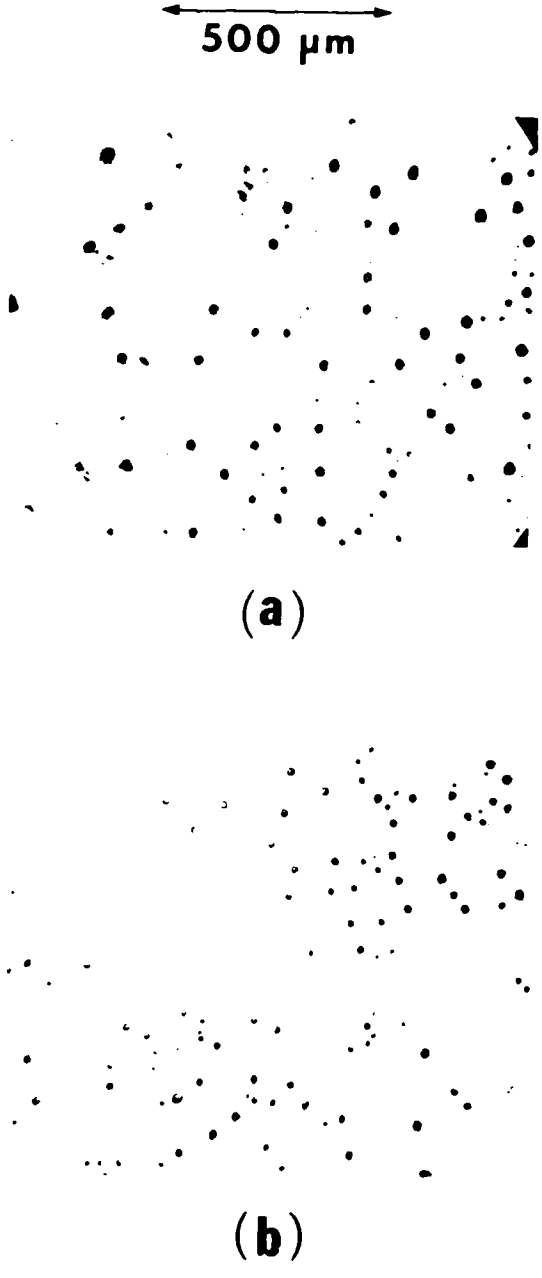


FIGURE 13. OPTICAL MICROGRAPHS SHOWING DEFECTS AT THE SURFACES OF CONTROL (UNANNEALED) AND ANNEALED Si_3N_4 CAPPED SAMPLES: a) Control; b) Annealed.

5. DEFECT GETTERING

To evaluate the gettering efficiency of back-surface-damaged wafers, we examined 50 samples prepared under a variety of experimental conditions. Since the required annealing cap was shown reproducibly to exert only a negligible effect on gettering of defects at the front surface, we assumed that all observable reductions could be primarily associated with strain introduced by defects at the opposite surface. In Figures 14 and 15, we show representative optical micrographs obtained at the front surfaces of control and back-surface damaged, annealed GaAs samples with (100) orientation, exposed to a pH controlled H_2SO_4:H_2O_2:H_2O (3:1:1) etch solution.

In Figure 14a), the control samples were coated with a 1000 Å plasma-deposited Si_3N_4 layer. After stripping the nitride layer in an HF solution, the samples were exposed to the (3:1:1) etch solution. Similarly, the sample in Figure 14b) was capped with Si_3N_4, and subjected to 30 seconds of mechanical damage using a 30-μm particle size and an 8000-rpm rotation rate. Subsequently, the sample was annealed at 800°C in flowing H_2 for 30 minutes and the cap removed in HF. After rinsing in DI water and drying, the sample was exposed to the (3:1:1) solution to reveal defect etch figures at the surface. The optical micrograph of the control sample shows an etch figure count of $\simeq 10^4/cm^2$, whereas after mechanically damaging the back surface and annealing, an etch figure density of $\simeq 90/cm^2$ is observed, representing a gettering efficiency of $\simeq$99.1%. In identical experiments on separate sets of samples, we obtained comparable efficiencies in the range, 92% to 97%.

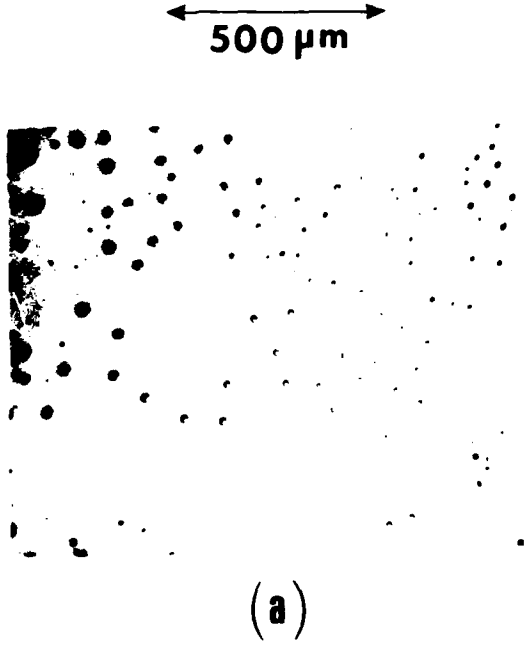
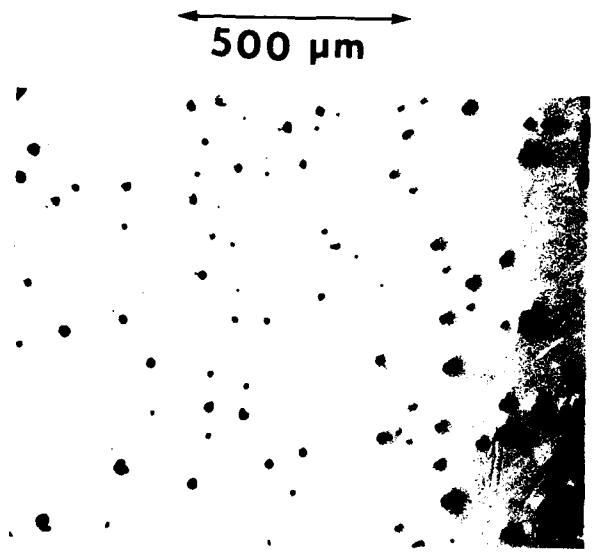


FIGURE 14. OPTICAL MICROGRAPHS OF FRONT SURFACES OF CONTROL AND BACK-SURFACE-DAMAGE GETTERED WAFER (30-µm PARTICLE SIZE, 8000 rpm, 30 sec); a) Control; b) Annealed, gettered.

In Figure 15, control and mechanically-damaged samples were treated in a similar fashion, except that the particle size was reduced to 0.3 m. The etch figure density in the control sample (Figure 15a)) is $\simeq 7 \times 10^3/cm^2$, whereas the etch figure concentration in the back-surface-damaged sample that was annealed is $\simeq 1.2 \times 10^3$, corresponding to a defect gettering efficiency of $\simeq 83\%$. Subsequent experiments showed good repeatability, with an average gettering efficiency of $\simeq 81\%$.

In all cases, we were able to demonstrate that the mechanical damage introduced in the back surface yields a significant improvement in substrate quality and reductions in defect concentration at the front surface of the wafer. Correlated TEM examination of samples exhibiting dislocation densities (etch figure counts) $\geq 10^4/cm^2$, showed similar reductions in defect density after damaging and annealing. However, in several cases, localized regions of high dislocation density were observed on control samples. Examinations of gettered samples obtained from the same wafer showed no apparent dislocation nests and a significant reduction in the number of dislocations intersecting the (100) surface.

In a correlated set of experiments, we implanted the back surfaces of 10 GaAs samples with 350 keV Ne ions to a dose of 10^{16} ions/cm^2. All implants were done at room temperature and the front surfaces capped with 1000 Å-thick Si_3N_4 layers. After annealing at 800°C for 30 min, the encapsulation layer was stripped and exposed to the surface etch. A defect density of $\simeq 6.6 \times 10^3/cm^2$ was observed on the unannealed control sample in Figure 16a). After annealing, the defect density at the front surface of the implanted sample decreased to $\simeq 1.7 \times 10^3/cm^2$ (Figure 16b), with an apparent gettering efficiency of 74%. In all samples examined, we were unable to obtain gettering efficiencies comparable to values routinely observed for the mechanically damaged samples. It is apparent that damage stability during thermal annealing is



(a)

(b)

FIGURE 15. OPTICAL MICROGRAPHS OF FRONT SURFACES OF CONTROL AND BACK-SURFACE-DAMAGE GETTERED WAFER (0.3-µm PARTICLE SIZE, 8000 rpm, 30 sec); a) Control; b) Annealed, gettered.

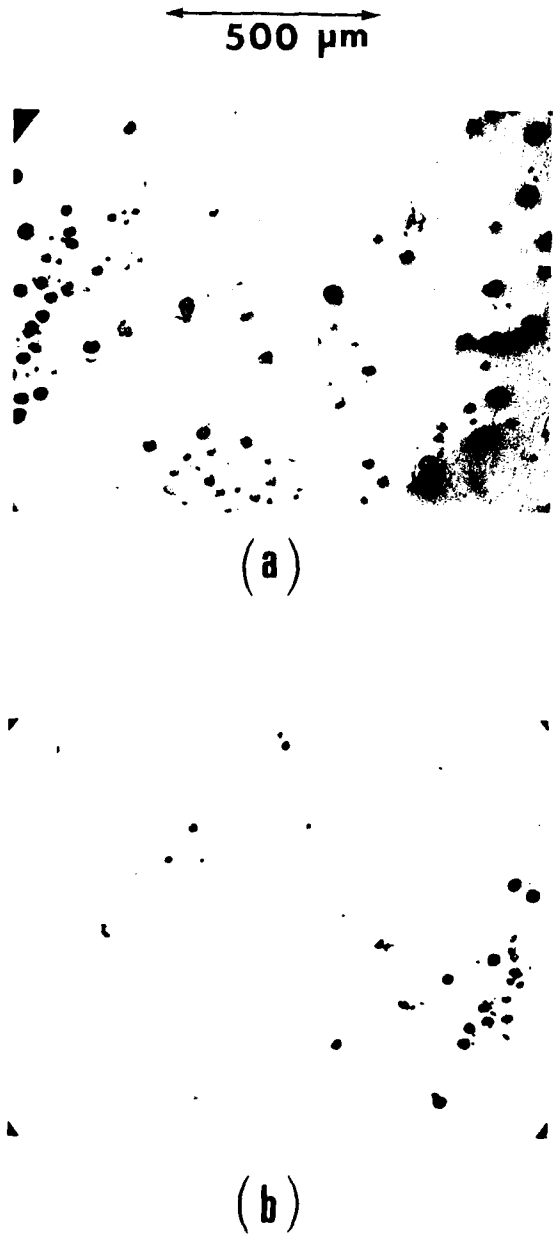


FIGURE 16. OPTICAL MICROGRAPHS OF FRONT SURFACES OF CONTROL AND ION-IMPLANTATION GETTERED WAFER; a) Control; b) Implanted (back surface), 350 keV Ne, $10^{16}/cm^2$, annealed 800°C, 30 min).

an important factor in defect gettering. To increase the effectiveness of ion-implantation gettering, it will be necessary to either increase the damage retention time or provide a graded damage profile by multiple implants of varying dose and energy.

6. GOLD IMPURITY GETTERING

Although a number of studies have shown that heavy metals and other impurities can be effectively gettered in Si by ion-implantation or mechanical damage, there have been no extensive invesigations on the gettering of Au and Cr by defects in GaAs. The purpose of these experiments was to determine if impurities can be gettered by defects introduced by mechanical damage at the back surface of GaAs wafers.

Silicon- and chromium-doped wafers of (100) orientation were obtained from Monsanto, Inc. and Crystal Specialties, Inc. Resistivities were of the order of 10^8 Ω-cm (Cr-doped) and $\simeq$ .008 Ω-cm (Si-doped). After cleaning and degreasing the wafer surfaces, specimens were exposed to rotary mechanical abrasion using particle sizes of 0.3 μm, 12.5 μm, 30 μm, and 60 μm. Experimental techniques were identical to those described in the previous sections. For gettering experiments, we coated the polished front surfaces with gold or chrome powder (99.99% purity) suspended in methanol. Afterwards, the samples were weighed to assure uniform concentrations for each experiment. Control samples (no back-surface damage) were similarly coated for comparative analysis. All samples were then annealed at 800°C for 30 min to one hour in flowing H_2.

Secondary ion mass spectroscopy (SIMS) and Cs-ion milling[16] were used to obtain impurity concentration profiles at the back surface of each sample. A gold-implanted sample was used to obtain both concentration and depth calibration for the annealed samples.

Figure 17 shows a plot of the log Au-ion intensity and concentration as a function of depth from the back surface for annealed samples damaged by rotary abrasion using particle sizes, σ, in the range, 0.3 μm to 60 μm. We observe that the maximum concentration of gettered Au atoms increases rapidly as a function of increasing particle size. For a particle size, 0.3 μm, the maximum Au concentration is located within a narrow near-surface region of width $\lesssim$ 500Å. However, for $\sigma \geq 30$ μm, the Au is distributed throughout the dislocation line region. In comparative studies of a number of control samples (no back-surface damage) containing Au at the front surface and annealed under similar conditions, we observe no Au at the back surfaces.

To determine the correlation of Au concentration and dislocation line density, we compared the integrated impurity and dislocation densities in the ratio:

$$\alpha = \int_{o}^{d} \frac{C(x)\ dx}{\rho(x)}$$

where $c(x)$ (cm^{-3}) is the concentration of Au as a function of depth, $\rho(x)$ (cm/cm^{-3}) is the measured dislocation line density in sectioned samples over the depth, d(cm) at the back surface (ρ = o). Calculations of α, then, provide a dimensionless number defining the number of impurity atoms associated with each dislocation line.

Figure 18 shows a plot of α versus particle size, using the previous equation and data from Figures 7 and 17. The graph illustrates a linear dependence of α and particle size. Since the dislocation density is proportional to the size of the abrasive particle, it can be inferred that the gettering efficiency is also proportional to the dislocation content at the back surface. When $\alpha = 1.5 \times 10^5$, there are approximately 10^5 Au atoms associated

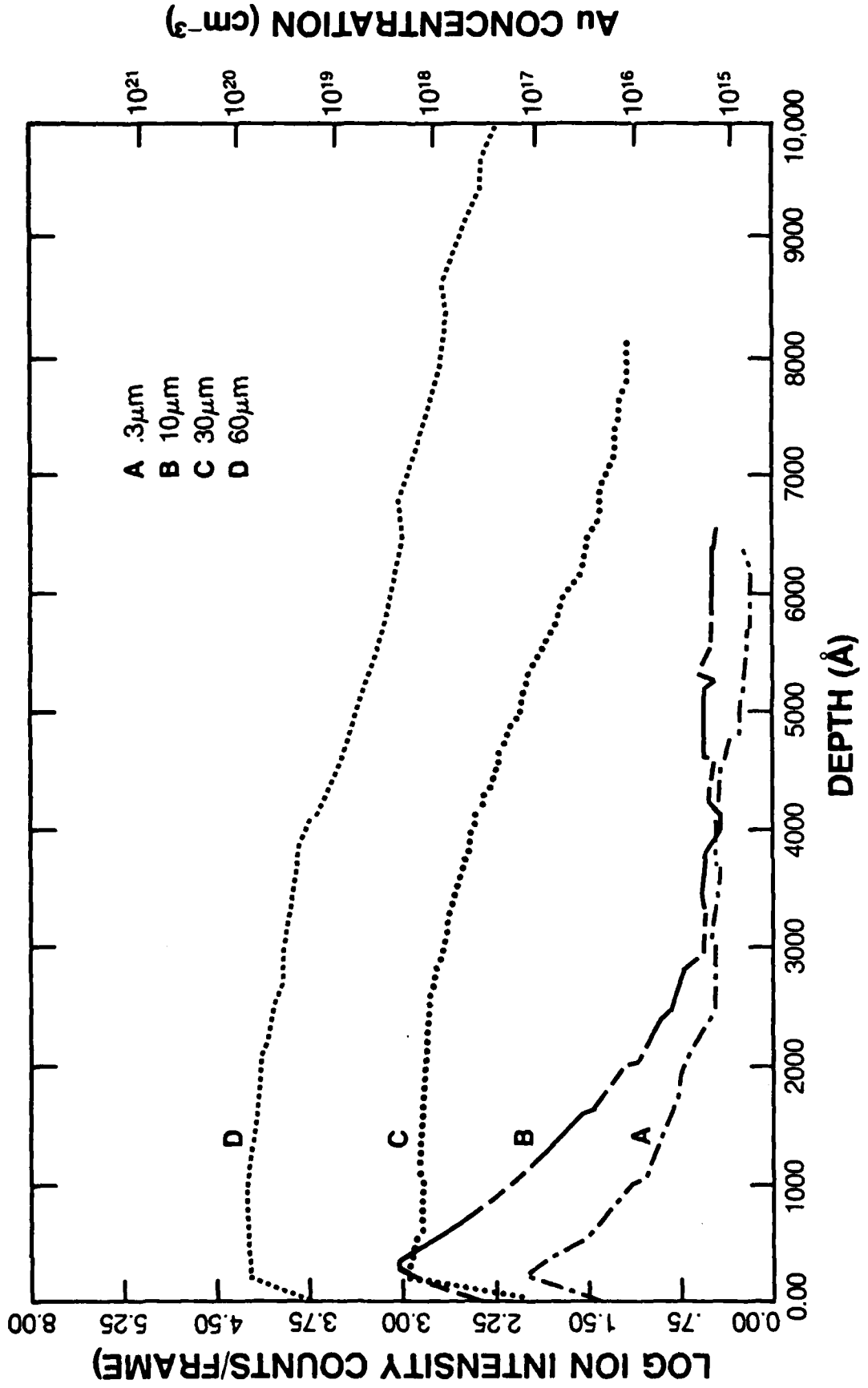


FIGURE 17. SIMS PROFILES OF Au AT BACK SURFACES OF DAMAGED WAFERS.

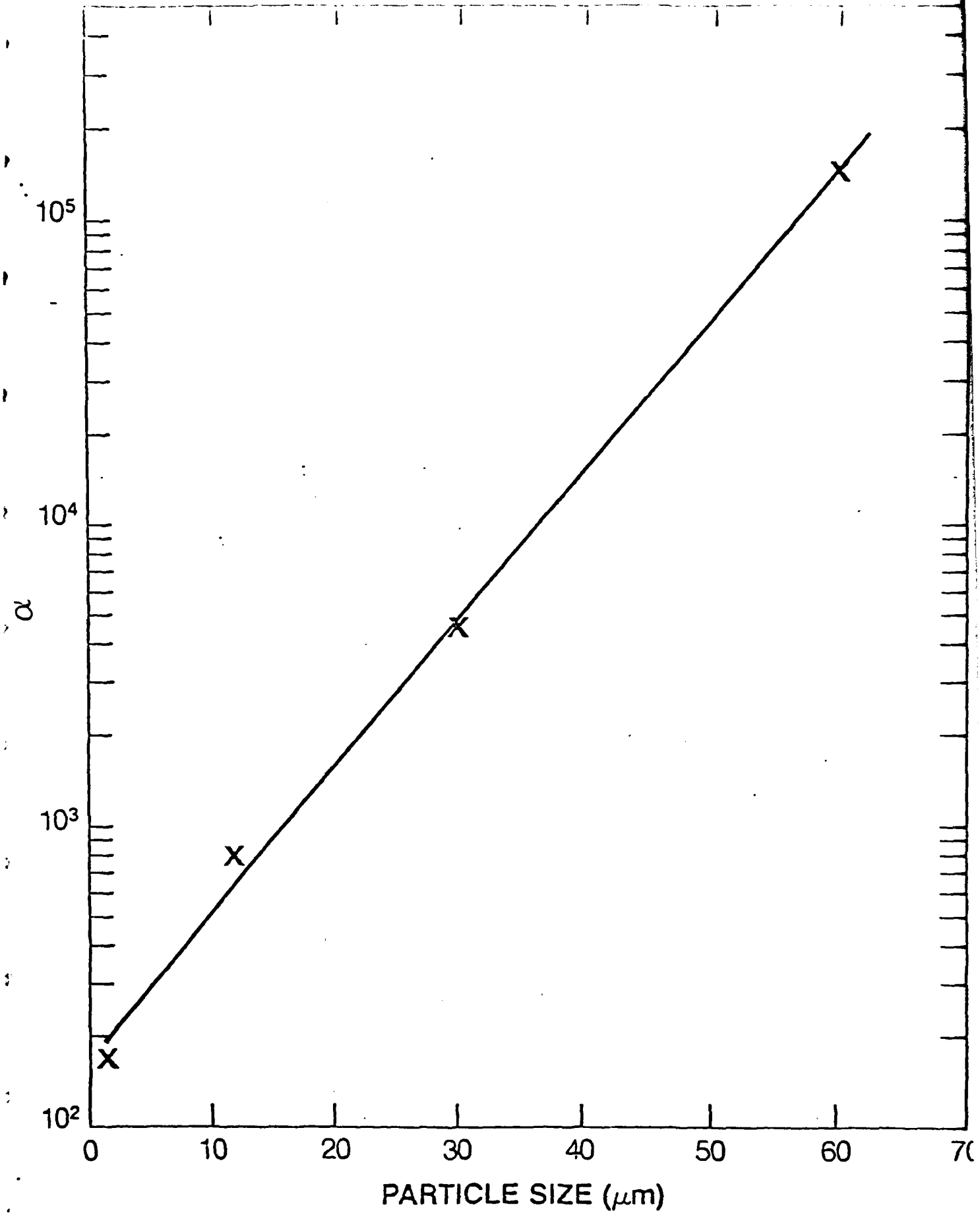


FIGURE 18. GRAPH OF α VS PARTICLE SIZE.

with each dislocation line at the back surface. For an average line length $\simeq 0.5\ \mu m$, there are then $\simeq 10^3$ sites available along the core of a dislocation line for trapping of individual impurity atoms. However, since $\alpha = 1.5 \times 10^5$, the number of Au atoms present greatly exceeds the available core sites for trapping, and the Au is not trapped along core sites but is present either in the form of impurity clouds surrounding dislocation lines or precipitates pinned at the edge of dislocations.

To obtain additional information on the possible location of Au in relation to microstructure at the back surface, we prepared annealed samples for TEM/TED analysis. For comparison, we also examined damaged (control) samples prepared under identical conditions but annealed with Si_3N_4 rather than Au on the front surface and undamaged (control) samples coated with Au and annealed. Figure 19 shows an electron micrograph obtained on a back-surface-damaged sample (σ = 60 μm, 8000 rpm, 30 sec) containing Au at the front surface after annealing for 40 minutes in flowing H_2. The presence of precipitates can be noted along the length of these dislocation lines in the bright-field micrograph shown in Figure 19. Corresponding dark-field micrographs also confirm the presence of Au on dislocation lines. In all samples examined, we detected similar decoration of the dislocation line structure by precipitates. In contrast, we observe no evidence of precipitation along dislocation lines in any of the control samples prepared and annealed in the same manner. We can, therefore, conclude that Au is present in the form of precipitates pinned along dislocation lines.

If, indeed, the Au is predominantly localized along dislocation lines, it would be interesting to estimate the number of Au atoms pinned along each line using TEM data. From a number of micrographs, the mean (image) diameter of precipitates was found to be $\simeq$ 100 Å. Assuming an actual diameter, $d_o \simeq$ 50 Å, and d_{Au}

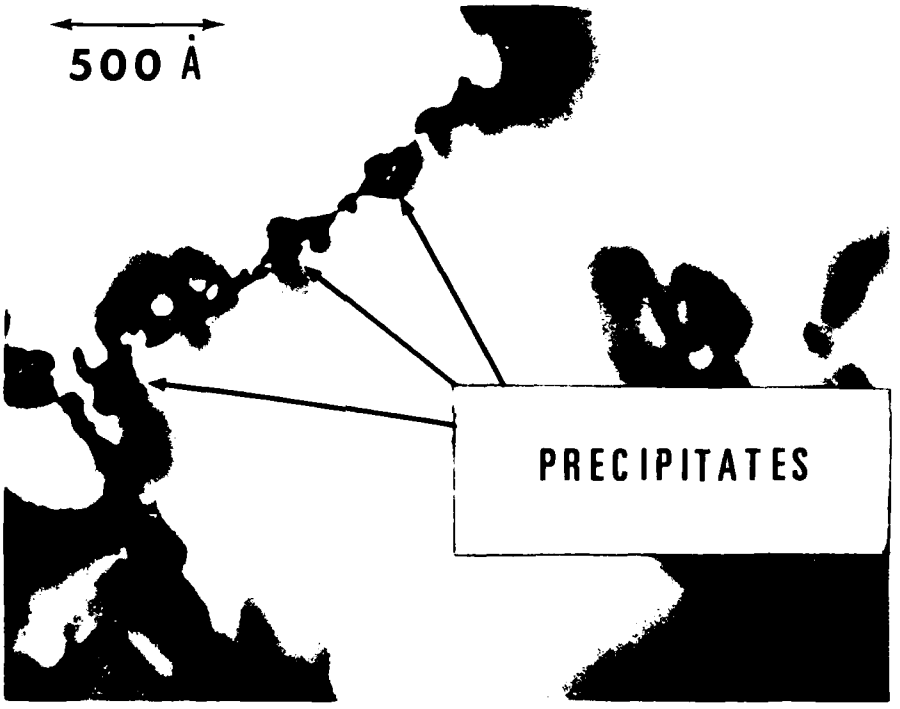


FIGURE 19. BRIGHT-FIELD ELECTRON MICROGRAPH SHOWING PRESENCE OF Au PRECIPITATES ALONG DISLOCATION LINES.

$\simeq$2.74 Å, the number of Au atoms contained in each precipitate region is $\lesssim 6 \times 10^3$. The mean number of precipitates per dislocation line was then determined and the Au concentration calculated to be $\simeq 0.95 \times 10^5$ atoms/line. In contrast to the corresponding value of $\alpha = 1.5 \times 10^5$ atoms/line calculated from SIMS and TEM data (Figure 18), we find reasonably good agreement, particularly in terms of the experimental uncertainties in adequately imaging all of the precipitates selectively pinned along dislocation lines.

Similar experiments were conducted on back-surface-damaged samples containing a Cr layer on the front surface. After annealing for 40 minutes at 800°C in flowing H_2, we observed detectable concentrations of Cr within the region containing dislocations. In Figure 20, we show representative AES spectral data obtained from the back surface at a depth of $\simeq$1000 Å. Chromium is clearly present at levels of $\simeq$ 0.7 atomic percent. At depths of 1 μm, Cr is still present, descreasing to concentrations below the detection capability of AES for depths > 1.2 μm. In the next section, SIMS profiling results will be presented, showing the distribution of gettered Cr as a function of depth.

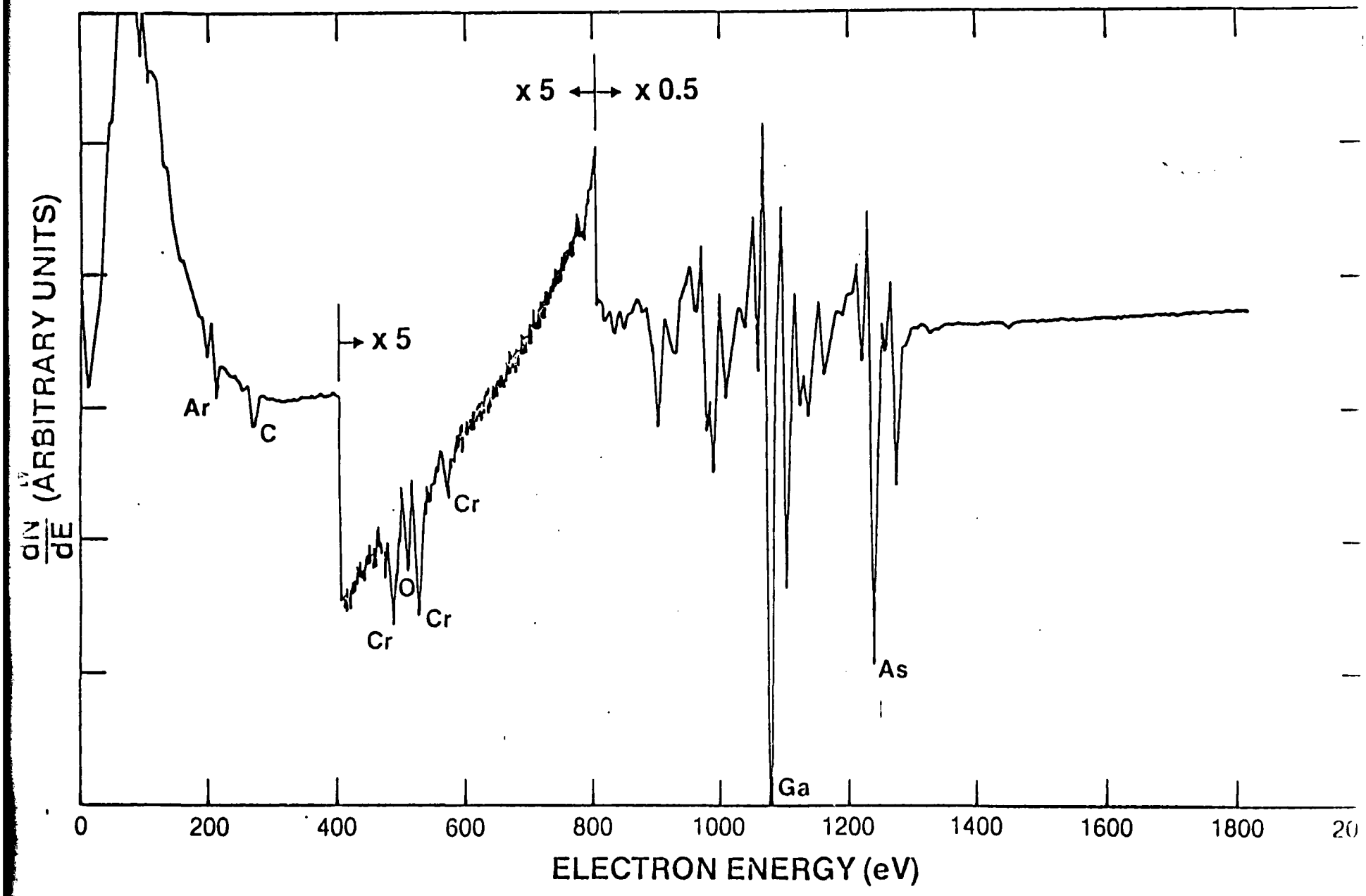


FIGURE 20. AES CHEMICAL DEPTH PROFILE OF BACK-SURFACE-DAMAGED WAFER AT DEPTH OF 1000 Å SHOWING THE PRESENCE OF Cr GETTERED BY DISLOCATIONS.

7. GETTERING OF Cr BY BACK-SURFACE MECHANICAL DAMAGE

Gettering of impurities in Si by ion-implantation-induced damage or mechanical damage has been reported[7,18-22] by a number of investigators. In contrast, there have been few detailed studies of impurity gettering by back-surface damage in GaAs. It has been shown[23] by the present authors that Au impurities could be effectively gettered by dislocation lines introduced into the back surface of GaAs wafers. The Au was observed in the form of precipitates pinned along dislocation lines that extended to a depth of $\sim$ 1.5 μm below the level of damage grooves at the back surface. Correlated transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) data showed the gettering process to be effective for annealing periods not exceeding the thermal stability time, or the time in which major microstructural damage is largely annihilated by annealing at a fixed temperature.

Preliminary studies by the authors have shown that Cr can also be gettered by mechanical or ion-implantation damage in GaAs.[24] The purpose of these investigations was to extend the previous studies and to determine the gettering behavior of Cr as a function of annealing duration for variable periods, approaching the thermal stability time at 800°C.

7.1 EXPERIMENTAL PROCEDURE

The galium arsenide samples used in these experiments were obtained from Crystal Specialities Inc. and Monsanto Corporation. The wafers were of (100) orientation ($\pm 1^{\circ}$) and doped with Si or Cr to levels of 0.008 Ω-cm and 10^{8} Ω-cm, respectively. Mechanical damage was introduced at the back surfaces using a 30- μm particle size and a rotary abrasive technique described elsewhere.[23]

All anneals were subsequently done in flowing H_2 at 800°C for periods of 0.5 to 6 hours. Samples for TEM analysis were prepared by conventional jet thinning and sectioning techniques on 2.5-mm x 2.5-mm specimens. Bright- and dark-field electron microscopy was used in all cases to examine the structure of control, damaged and annealed samples.

Secondary ion mass spectrometry was used to obtain Cr impurity concentration profiles at the back surfaces of control and back-surface-damaged, annealed samples. To obtain calibration data for these experiments, GaAs and Si samples were simultaneously ion implanted with Cr and the integrated Cr content measured in the Si by nuclear back scattering techniques.[25] These data were then used to convert the measured Cr signals from SIMS profiles on GaAs and the resulting data correlated with predicted LSS (as-implanted) profiles.

7.2 RESULTS

7.2.1 TRANSMISSION ELECTRON MICROSCOPY

Samples were subjected to rotary back-surface abrasion using a 30-μm particle size, 8000-rpm rotation rate and a total contact time of 30 sec. Specimens were then examined in the electron microscope and micro-structural damage found in the form of laterally continuous forested dislocation nests extending to a distance of $\sim$ 1.5 μm below the depth of damage grooves at the back surface, in agreement with previous results.[23]

Dislocation line structure was observed to be largely annealed after heating for 2 - 3 hours in flowing H_2 at 800°C. Some residual dislocation line structure was found to persist up to anneal periods of 6 hours, but the fractional amount of damage remaining after 3 hours was typically $\leq$10% of the initial dislocation line content.

Figure 21 shows a series of bright-field electron micrographs obtained at the back surfaces of Cr-doped samples subjected to back-surface damage and subsequently annealed at 800°C for variable periods. It can be observed that the concentration of dislocation lines is considerably reduced as a function of increasing anneal time. Of particular importance, however, is the apparent absence of any identifiable precipitates or impurity segregation sites, either at the edges of dislocation lines or in isolated zones. This result is in sharp contrast to the previous result in which Au was shown reproducibly to nucleate in the form of precipates pinned along dislocation lines. In all cases, we were unable to clearly identify precipitates in the back-surface-damaged and annealed Cr-doped samples. From these results, we can infer an absence of Cr precipitation along dislocation lines or a relatively weak strain field from small Cr segregation zones that do not permit adequate resolution by TEM.

To further investigate the possibility of Cr precipitation within the damaged regions, a series of experiments was conducted on selected Si-doped samples shown by SIMS to contain small (unintentional) Cr-doping concentration of $\leq 10^{16}$ cm^{-3}. Chromium layers of 2-μm thickness were then deposited on the front surfaces by an electroless technique and the uniformity checked by SEM examination. The samples were then heated in flowing H_2 at 800°C for variable periods, as in the previous experiments, and the samples examined at the back surface in the TEM. The micrographs obtained were essentially identical to those shown in Figure 21 and no Cr precipitation was detected, although gettered Cr was clearly detectable by SIMS, as will be discussed in the next section.

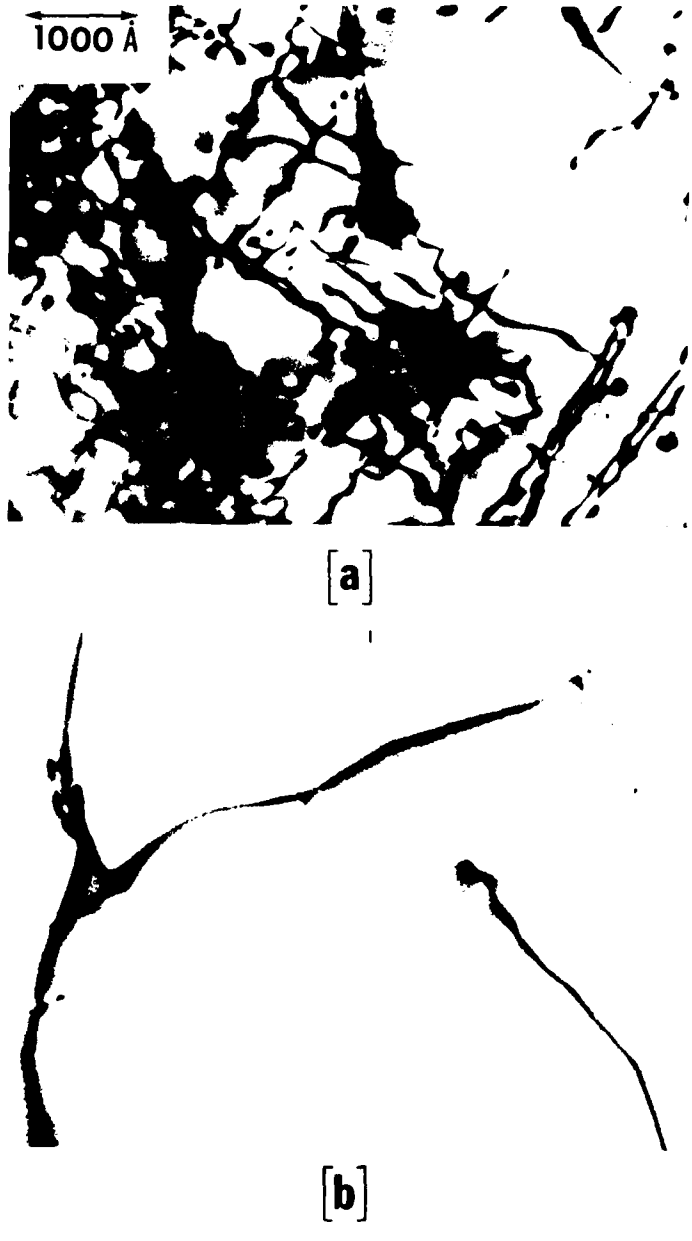


FIGURE 21. TRANSMISSION ELECTRON MICROGRAPHS OF BACK-SURFACE-DAMAGED WAFERS AFTER ANNEALING; a) 30 min.; b) 180 min.

7.2.2 SECONDARY ION MASS SPECTROMETRY

Figure 22 shows SIMS profiles obtained at the back surface of Cr-doped control and mechanically-damaged GaAs samples subjected to anneals at 800°C for variable periods. Also shown for comparison is a representative profile obtained from an annealed, Si-doped (back-surface-damaged) GaAs sample containing a $\sim$2-μm thick Cr layer on the front surface. All SIMS profiles were obtained within homogeneous damage distribution zones at the back surface.

Control (undamaged) samples subjected to 800°C anneals typically show a narrow region of Cr accumulation at the back surface. This is presently thought to be attributable to a slight gettering effect caused by the presence of small amounts of residual defect structure retained after chemical/mechanical polishing. After annealing of the back surface damaged samples for 1/2 hour, we observe a significant concentration of Cr at the back surface. For all samples, we detected a graded distribution,decreasing to background doping levels at depths of $\sim$1.5 μm. After annealing for 2.5 hours, the level of gettered Cr is reduced and the concentration gradient decreased. For anneal times >2.5 hours, no additional reduction in Cr concentration is observed, and SIMS profiles are essentially identical to the results obtained at 2.5 hours.

For comparative purposes, we conducted a series of experiments on carefully selected Si-doped wafers shown by SIMS profiles to contain small concentrations of Cr. Layers of Cr were then deposited on the front surfaces of both control and back-surface-damaged samples and the specimens annealed at 800°C. Evidence of near-surface Cr gettering was observed at the back surfaces of control samples. In contrast, large accumulations of Cr were observed in back-surface-damaged samples annealed for comparable periods at 800°C (Figure 22), always exceeding the concentration for control samples. In agreement with the previous results, the

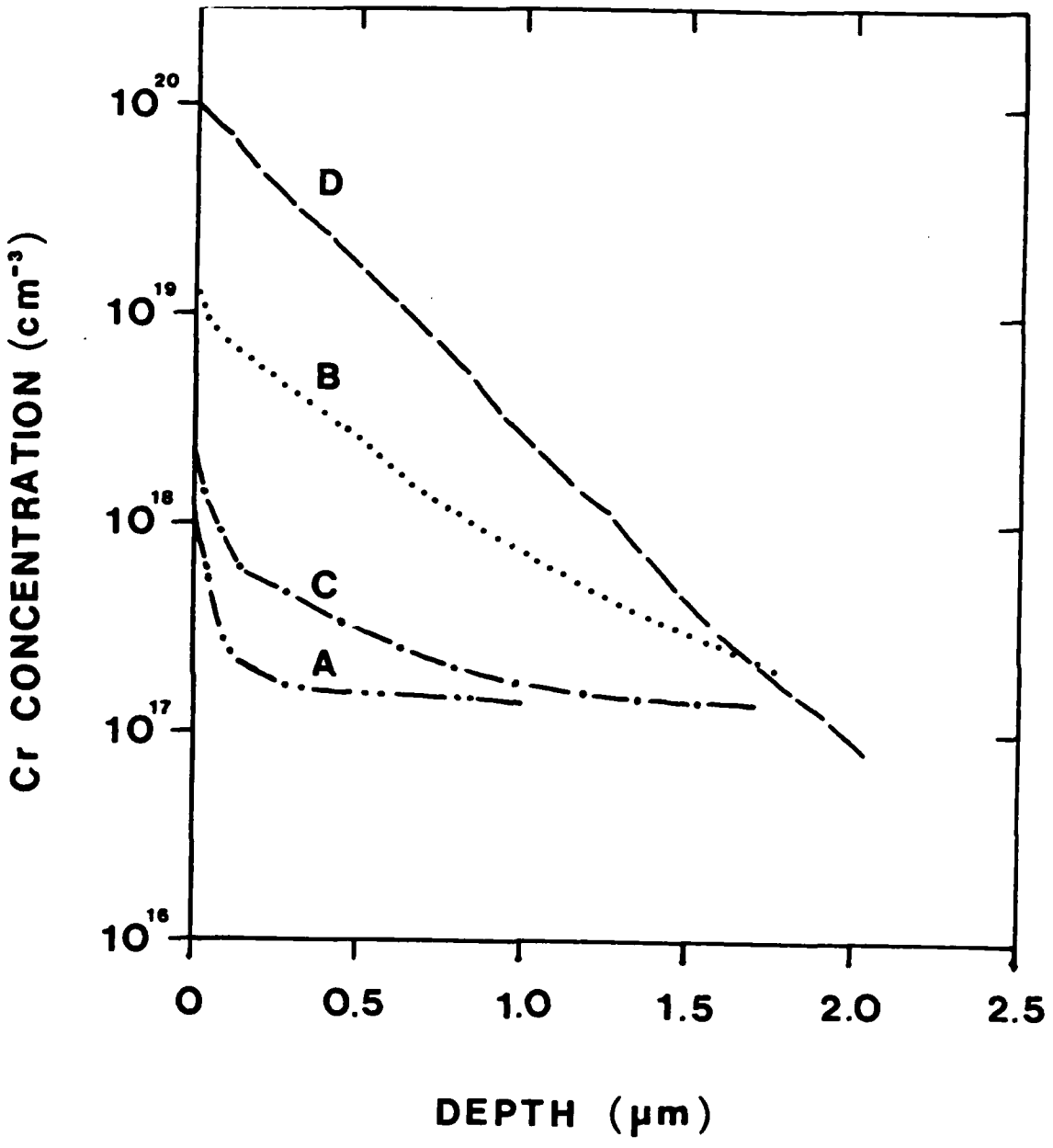


FIGURE 22. SIMS PROFILES OF BACK-SURFACE GETTERED Cr IN GaAs WAFERS; a) Control (no induced damage), Cr-doped, annealed 800°C, 1 hr; b) Cr-doped, annealed 800°C, 0.5 hr; c) Cr-doped, annealed 800°C, 2.5 hr; d) Si-doped, Cr layer (front), annealed 800°C, 1 hr.

gettered Cr was detected with a $\sim$ 1.5-μm thick zone at the rear surface of the sample.

From the data obtained, we observe that the gettered Cr is positioned within a zone approximately equal to the depth of the distributed dislocation line structure at the back surface, as determined by TEM. The Cr concentation is also graded, approximately following the dislocation line gradient found in TEM measurements.[23] At short annealing times ($\leq$1 hr) the gettered Cr is relatively stable at the back surface, whereas for annealing periods > 1 hr, the concentration of Cr is reduced as a function of increasing anneal duration. This reverse annealing or "degettering" effect can be directly correlated with the annealing of dislocation line structure reported in reference 23. As the damage is gradually annihilated with increasing anneal time, Cr is released and allowed to move back into the interior of the wafer. After 2.5 hours of annealing, the Cr concentation is relatively stable and no further modifications in SIMS profiles are observed. For anneal periods > 2.5 hours, dislocation lines are also largely annihilated and only small concentrations of residual defects remain at the back surface.

The gettering of Cr from the front surface is also directly related to the presence of dislocation line structure at the back side of the wafer. This anomalous diffusion of Cr may be related, in part to the motion of As vacancies released from the damaged region during annealing, or to the direct interaction between the strain field at the rear surface and Cr impurities at the front (or both). None of the experiments revealed the precipitation of Cr in discrete zones or pinned sites along dislocation lines. The results suggest that the gettered Cr is present either in substitutional sites or in complexes not readily resolvable by TEM techniques.

To extend this study, we conducted a series of experiments in which a 2-μm CVD SiO_2 layer doped with As to a level $\simeq 10^{20}$ atoms/cm^3 was used as an encapsulant at the rear surface of the back-surface-damaged wafer. It was found by TEM that the damage thermal stability time at temperatures in the range 700°C to 830°C could be increased by a factor of two, resulting in an apparent maximum of 4 hours available processing time at 800°C. As in the earlier investigations, annealing times in excess of the thermal stability time caused pronounced damage annihilation at the back surface.

To further supplement these data, the thick SiO_2 caps were removed after annealing and SIMS profiles measured to ascertain the effect on Cr gettering. Using 30-μm particles in the rotary abrasive damage procedure, we found that Cr was rapidly gettered after 0.5 to 1 hour of annealing at 800°C. For annealing times exceeding 2.5 hours, we found pronounced de-gettering, or reverse annealing of Cr, corresponding to the point at which damage annealing is pronounced at the back surface. In comparison to the results shown in Figure 22, however, reverse annealing is considerably altered and a longer period of time present before the mobile Cr is degettered and allowed to diffuse back into the interior of the GaAs wafer.

8. BACK-SURFACE GETTERING AND Cr OUTDIFFUSION IN VPE GaAs LAYERS

Semi-insulating (Cr-doped) gallium arsenide has been widely used as a substrate material for the growth of epitaxial layers in fabricating microwave FET structures. To improve the performance of such devices, a buffer layer is commonly inserted between the substrate and active layer to reduce the outdiffusion of impurities into the active layer and to isolate the effects caused by defects propagating into the film at the substrate-epitaxial layer interface.[10] Recent experiments by Tuck et al.[17], using radiotracer techniques, showed that Cr diffuses readily into VPE layers during epitaxial growth at substrate temperatures in the range 745°-750°C. Their data suggested that the rapid diffusion and an interstitial diffusion mechanism must be invoked. Separate experiments, using secondary ion mass spectrometry (SIMS) and transmission electron microscopy/diffraction (TEM/TED) on Ne ion-implanted or mechanically-damaged back surfaces of GaAs wafers[24,27], have also shown rapid motion and subsequent gettering of Cr at 750°-800°C for anneal times in the range 0.5-1 hour, thereby lending additional support for a non-substitutional diffusion mechanism.

The concentration of point defects and dislocation lines at the substrate-epilayer interface will exercise an important influence on the outdiffusion of Cr and other impurities into the epitaxial layer. Improvements in the quality and microstructural defect content of epitaxial GaAs layers have been previously noted when back-surface-damaged, pre-gettered substrates were used.[6,28] However, to our knowledge, there have been no reports of the effect of (substrate) damage pre-gettering on the outdiffusion of Cr into epitaxial layers during growth. In the next sections, correlated data from TEM and SIMS measurements are presented which show the influence of substrate gettering on the interfacial defect density and distribution of Cr in VPE layers during growth and subsequent annealing.

8.1 EXPERIMENTAL PROCEDURE

The semi-insulating GaAs wafers used in this study were obtained from two independent suppliers and were Cr-doped to achieve resistivities greater than 10^7 ohm.-cm. The wafers were typically oriented 3^o off the (100) toward the (110) and were polished on one side.

After cleaning, the polished front surfaces were coated with 2000 Å of SiO_2 deposited in a commercial pyrolitic decomposition reactor at 400^oC. The oxide film served as a scratch protection layer during back-surface-damage operations. A rotary abrasive unit was used to create macroscopic, concentric damage grooves ($\leq$ 30 µm) at the back surface of the wafer. After completion of the damage process, the SiO_2 layer was removed and a 1000 Å thick Si_3N_4 encapsulant formed on the front surface at 200^oC by plasma deposition. Anneals were done in flowing H_2 at temperatures in the range 750^o-900^oC.

Following the anneal, the Si_3N_4 film was removed and the wafers loaded into a vapor phase epitaxial reactor and heated to the deposition temperature of 720^oC. After a brief vapor etch, undoped epitaxial "buffer" layers were grown on both gettered and control wafers in the same run. The GaAs buffer layers were grown using a standard hydride (AsH_3+HC +Ga) reactor typically utilized for growing epitaxial material (active/buffer) for GaAs MESFET requirements.

Following epitaxial growth, samples were prepared for TEM/TED analysis by conventional jet-thinning techniques and examined in the microscope using bright- and dark-field electron microscopy. SIMS profiling was done in a Cameca IMS-3f ion microanalyzer. To obtain maximum Cr sensitivity, O_2+ bombardment was combined with positive secondary ion mass spectrometry. The Cr concentration

levels were determined using standards prepared by ion implanting Cr into both epitaxial layers and semi-insulating GaAs substrates.

8.2 RESULTS

TEM examination of back-surface-damaged samples showed that the rotary abrasive technique produces a heavily-forested, laterally-continuous array of dislocations extending to a depth of $\sim$ 1.5 μm below the depth of damage grooves at the back surface. Figure 23 shows a plot of the measured dislocation line density as a function of depth from the back surface. Also shown for reference is a SIMS profile of the Cr concentration at the back surface before and after annealing at 750°C for 1 hour. No significant dislocation line structure was observed in any sample at depths >1.5 μm. Correspondingly, the gettered Cr is concentrated within a region approximately equal to the width of the damage region. TEM examinations of the annealed samples show no evidence of precipitation along dislocation lines or in discrete segregation zones, suggesting that the Cr is present either in the form of complexes or regions not readily detectable by conventional TEM techniques.

To further investigate the effect of gettering at the front surface, we annealed for 1 hour at 750°C both control (no back-surface damage) and back-surface-damaged samples. A low-temperature (200°C) plasma-deposited Si_3N_4 layer (1000 Å thick) was used as the encapsulant. The Si_3N_4 encapsulants were removed and samples immersed in a H_2SO_4:H_2O_2:CH_3COOH(3:1:1) solutuion for 2 minutes.

Figure 24 shows optical micrographs of the front surfaces of annealed control (Figure 24a) and gettered (Figure 24b) substrates after immersion in the etch solution. The number of etch figures is considerably reduced in the gettered sample while the control samples consistently showed a density $\geq 2 \times 10^4/cm^2$. These experiments were then repeated for a number of samples with essentially identical results.

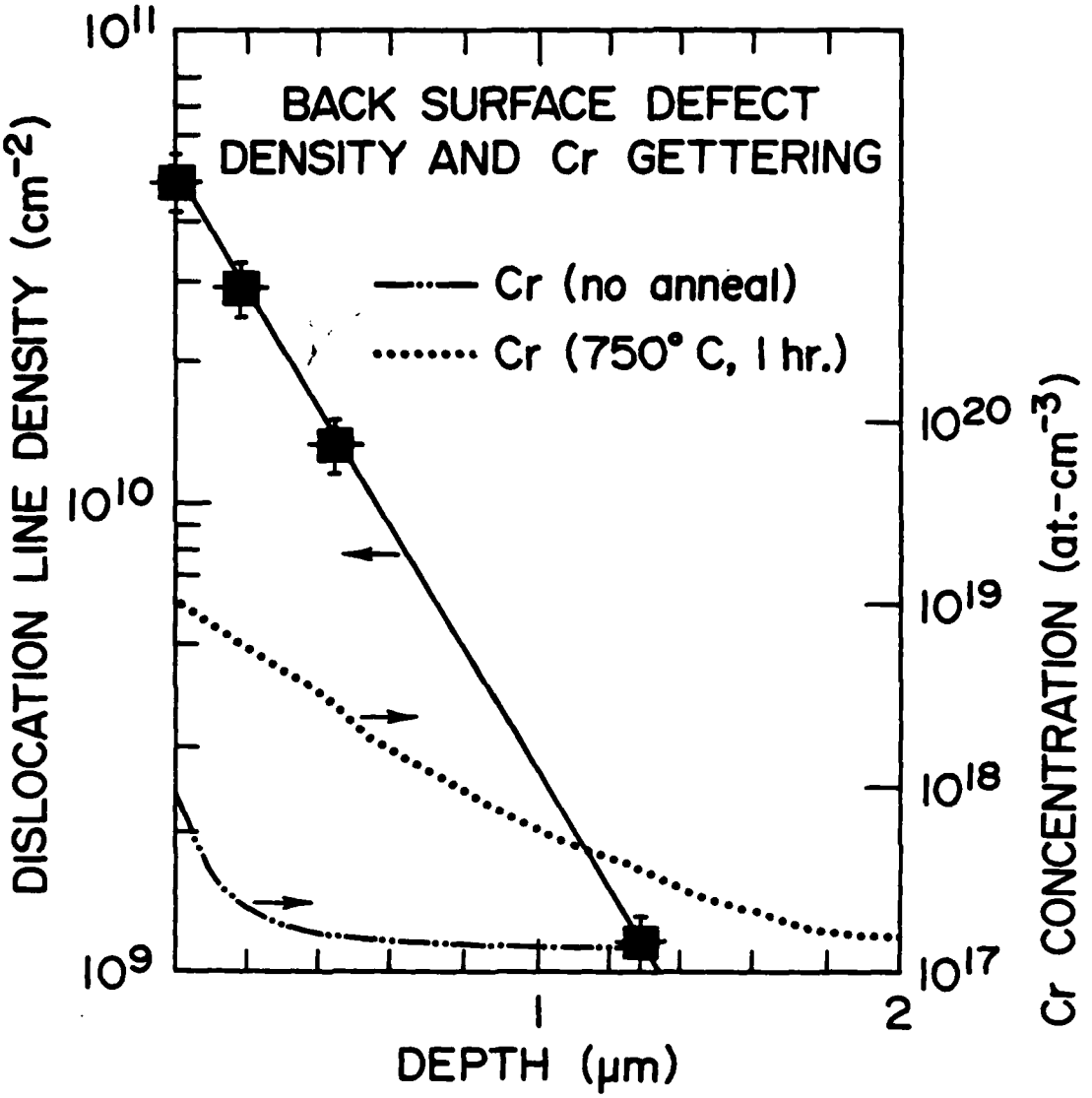
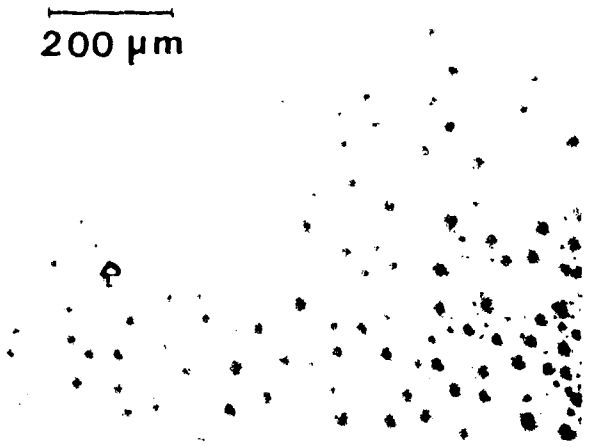
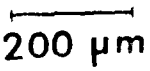


FIGURE 23. DEFECT DENSITY AND Cr CONCENTRATION PROFILES OF BACK-SURFACE-DAMAGED ANNEALED GaAs SUBSTRATES.



(a)



(b)

FIGURE 24. OPTICAL MICROGRAPHS OF ETCH FIGURES OF ANNEALED SAMPLES: a) Control; b) Gettered.

Correlated TEM examinations of the front surfaces also showed a reduction in substrate dislocation line density after gettering. To isolate any possible capping effect, unannealed and annealed control (capped) samples, prepared under similar conditions were examined and no appreciable reduction in defect density was observed. Examination of VPE layers grown on gettered and ungettered substrates was drastically reduced, essentially in agreement with the results of Schwuttke and Yang[28] on epitaxial GaAs layers grown on gettered substrates which were mechanically damaged at the back surface by impact sound stressing.

To determine the influence of gettering on Cr redistribution, SIMS measurements were made to obtain Cr concentration profiles on the substrate and epitaxial layers. Figure 25 shows SIMS profiles of the ^{52}Cr concentration in VPE layers on gettered and ungettered substrates after deposition and annealing. Figure 25a) shows that Cr has outdiffused rapidly during deposition in layers grown on both gettered and control (ungettered) substrates. However, the level of outdiffused Cr is significantly higher for the epitaxial layer on a control substrate. In all samples examined, the level of Cr was found to be reduced in VPE layers grown on pre-gettered substrates.

Figure 25b) shows the ^{52}Cr distributions in post-deposition annealed (800°C, 30 min.) VPE layers grown on gettered and ungettered (Si_3N_4 capped) substrates. The data suggest that the total Cr content in the VPE layer grown on the ungettered substrate is considerably greater than the Cr content in the epilayer grown on the pre-gettered substrate. Comparing Figures 25a) and 25b), it can be seen that the outdiffusion of Cr is suppressed in the pre-gettered sample whereas the Cr in the control substrate moves rapidly through the layer to the surface of the sample. The apparent near-surface pileup of Cr in both samples is thought to be a strain-induced effect caused by thermal mismatch between the encapsulant and the GaAs epilayer.[12]

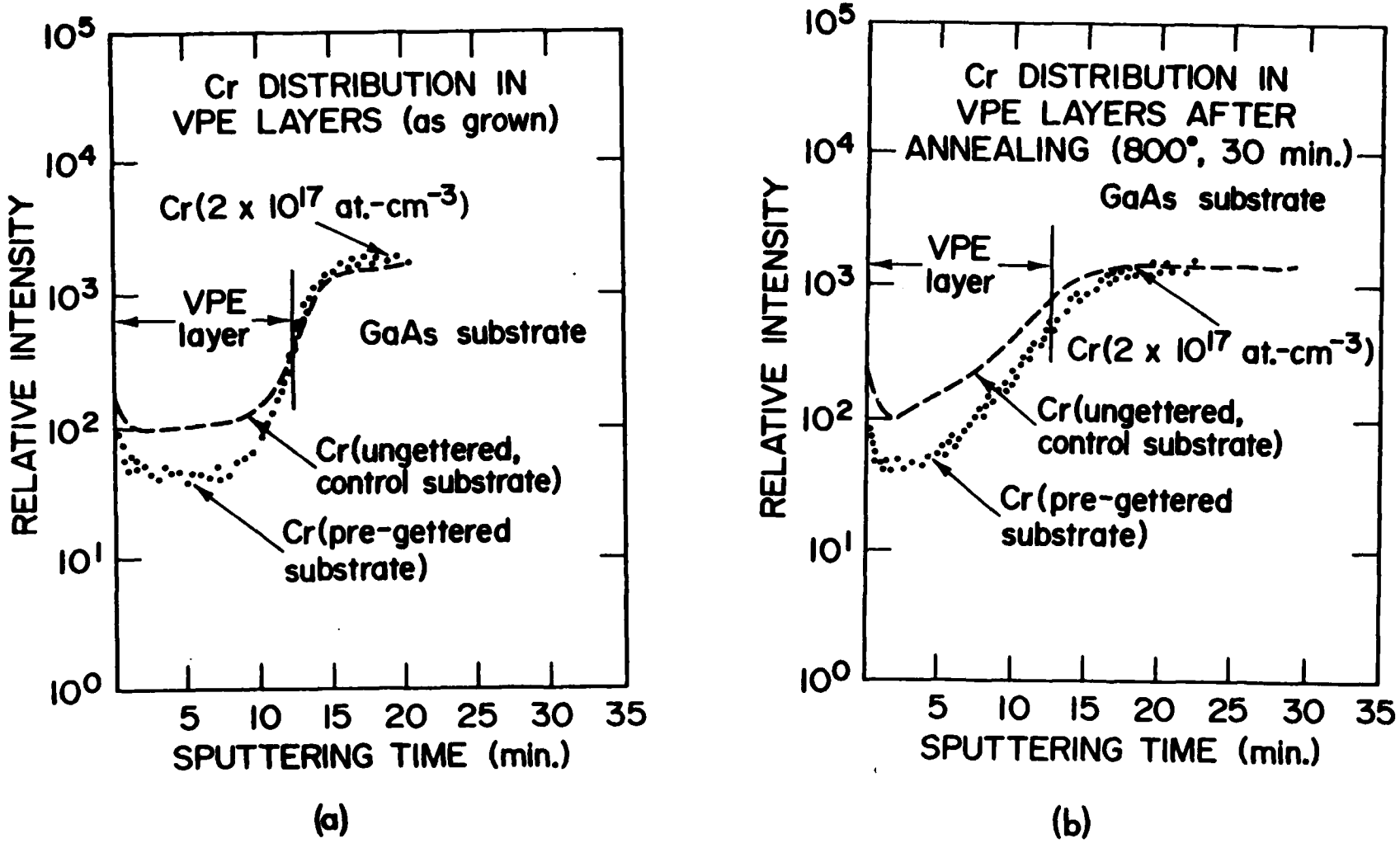


FIGURE 25. SIMS PROFILES OF Cr CONCENTRATION IN SUBSTRATES AND VPE LAYERS AFTER DEPOSITION AND ANNEALING: a) After deposition; b) 800°C post-deposition anneal (t_{VPE}=1.7μm).

Annealing at temperatures $\geq 850^{o}C$ produces significant Cr diffusion into VPE layers with no noticeable difference between profiles obtained on control or pre-gettered samples. TEM examinations of gettered samples annealed at higher temperatures also show that the back-surface damage is progressively annihilated as a function of increasing temperature and anneal duration. It can then be speculated that the removal of back-surface damage and strain gradients, caused by the presence of a graded dislocation line density (Figure 23), will correspondingly remove any apparent suppression of Cr outdiffusion from the substrate into the epitaxial layer.

From the data obtained, we can conclude that back-surface-damage gettering reduces the concentration of microstructural defects at the substrate surface and within the epitaxial layer. Since both point defects and line defects will contribute to enhanced diffusion of an impurity, the outdiffusion of Cr will be reduced during growth of VPE layers on pre-gettered substrates. During post-deposition annealing, the presence of a strain field gradient, produced by the dislocation line density at the back surface, will partially suppress the outdiffusion of Cr and will be effective until back-surface damage is annihilated at high-temperature anneals.

9. ALLOYING OF Au LAYERS AND REDISTRIBUTION OF Cr IN GaAs

The increasing utilization of GaAs as a material for fabricating microwave field effect transistors (FET), Gunn-effect diodes, and IMPATT diodes has, over the past 15 years, prompted a number of investigations on the annealing behavior of contact structures. In particular, the alloying characteristics of Au-Ge and Au-Ge-Ni structures on n-type GaAs have been widely reported,[29-37] but the problems of thermal aging and the processes which create high resistivity layers near the surface have yet to be satisfactorily resolved.[38-40] The deterioration of contact regions has in the past been ascribed to the indirect effects of strain-induced damage at the interface,[40-41] or to compensation of the Ge dopant by acceptors associated with As vacancies.[38]

Recent studies on VPE layers grown on Cr-doped (semi-insulating) GaAs substrates have shown that Cr out-diffuses readily into the epitaxial layers during deposition and annealing.[17,42] Another investigation has shown that Cr is rapidly gettered into the region of residual damage and interface of Se-implanted (capped) GaAs substrates, suggesting a possible correlation between Cr redistribution and the development of high resistivity layers at the surface after annealing.[38]

To our knowledge, there have been no reported studies of the effect of contact alloying on the redistribution of Cr at annealing temperatures in the range, 350-370°C. In this section, data from transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS) measurements are presented which show the development of damage structure and redistribution of Cr in n-type LPE layers and semi-insulating substrates after alloying thin Au films at 350°C for varying anneal times.

9.1 EXPERIMENTAL

Semi-insulating GaAs wafers used in this study were of (100) orientation and Cr doped to obtain resistivities $>10^7$ Ω-cm. The LPE layers (0.5-μm thick) on semi-insulating substrates were Sn doped to levels of $1x10^{17}$ atoms cm^{-3}. Gold films were vapor deposited at room temperature on cleaned samples at initial vacuum levels $<10^{-8}$ Torr. Annealing was done at 350°C in a flowing H_2 environment. In all cases, samples were rapidly removed from the furnace after annealing and placed on a heat sink to achieve fast cooling rates.

After the removal of Au layers, specimens were prepared for TEM analysis using standard jet thinning techniques and examined in the microscope. SIMS profiling was performed with a Cameca IMS-3f ion microanalyzer. The SIMS depth profiles used O_2 primary ion bombardment and positive secondary ion spectroscopy. The $^{71}Ga_2^{+1}$ molecular ion (designated ^{142}Ga in the figures) was used to establish the Ga-concentration profile since the singly-charged Ga^+-ion yield was too intense to measure with the electron multiplier. The Cr atomic concentration was calibrated using a $^{52}Cr^+$-ion implant into GaAs.

9.2 RESULTS

To examine initial defect content in substrate and LPE layers, we immersed samples in a H_2SO_4:H_2O_2:CH_3COOH(3:1:1) solution for 2 min. Optical microscopy examination showed surface defect densities $\simeq 2x10^4$ cm^{-2} in all samples tested. After deposition of Au layers, we removed the films and again etched substrates and LPE layers. The results showed no appreciable change in defect density, indicating that no dramatic increases in defect density are produced in these experiments by Au deposition alone.

Since etching experiments cannot adequately be used to reveal individual dislocation lines on alloyed surfaces, we used TEM analysis on both alloyed and control samples to obtain additional information on microstructure induced as a result of the alloying process. After Au deposition and subsequent annealing, we found a complex array of dislocations in the form of nests and tangles (Figure 26). In contrast, we found no evidence of such arrays in control substrates or unannealed Au/GaAs structures. Annealing for periods up to 10 min. at 350°C appeared to increase the amount of damage in direct proportion to the annealing time, essentially in agreement with earlier results of Gyulai et al.[37] obtained by back scattering. Annealing of 4000 Å-thick Au films for comparable periods produced a significant increase in dislocation density, suggesting that the defect density induced by alloying is directly proportional to the initial film thickness.

Examination of samples with deposited Au films of 1000 Å thickness of LPE layers also showed the same pattern of complex dislocation net works as shown in Figure 26 after annealing at 350°C for 1 minute. In like manner, additional alloying time increased the amount of damage present within the epitaxial layer.

Recent studies of Cr gettering in GaAs[27,42] have shown that Cr can exceed solid solubility in regions containing large amounts of crystalline damage without inducing additonal microstructural damage in the lattice. From these results and earlier investigations of damage induced in GaAs as a result of Au alloying, we can conclude that the observed damage in these experiments is associated with Au diffusion into the GaAs during alloying and not correlated with any Cr redistirubtion.

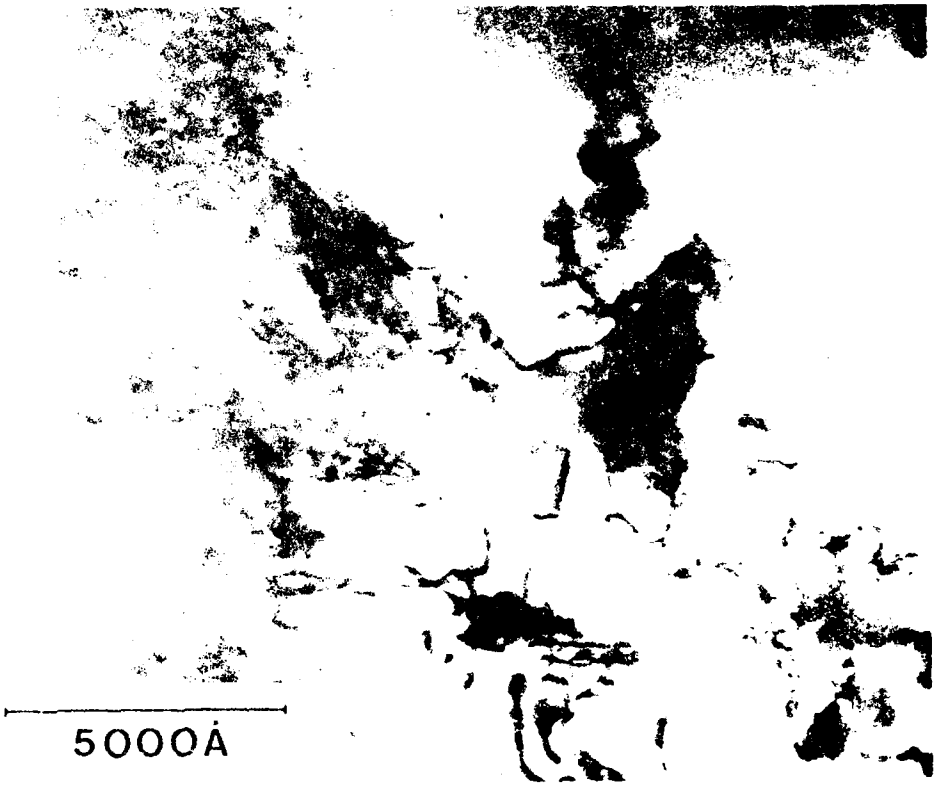


FIGURE 26. TRANSMISSION ELECTRON MICROGRAPH OF GaAs UNDER ($1000\ \text{Å}$ thick) Au CONTACT LAYER AFTER ANNEALING AT $350^{\circ}C$ FOR 1 MINUTE.

To obtain the in-depth data on the distribution of Cr within the substrate and Au film, we used SIMS profiling. In Figure 27, we show chemical profiles of an Au/GaAs structure after deposition of a 1000 Å-thick Au layer and annealing at 350°C for periods of 1, 3, and 10 min. In Figure 27a), we observe that after 1 min. of annealing, the Au has diffused into the GaAs substrate, accompanied by outdiffusion of both Ga and As through the Au layer to accumulate on the surface of the film. These results are in general agreement with earlier studies using Auger electron spectroscopy profiling.[34,43,44] Of particular importance is the near-surface pileup of Cr and subsequent outdiffusion from the substrate onto the surface of the Au film. In all samples examined, we observed similar pileups of Cr within the substrates near the interfacial region. For comparison, we also obtained SIMS profiles on unannealed Au/GaAs structures and found no evidence of Cr interfacial pileup or outdiffusion after deposition. After 3 min. of annealing (Figure 27b), the concentration of Cr is reduced in the near-surface region and outdiffusion into the Au film is further increased. Ten minutes of annealing produces substantial outdiffusion of Ga (Figure 27c) and an apparent annihilation of the sharply defined "knee" in the Cr distribution profile, observed in Figure 27a).

Similar experiments conducted on Sn-doped LPE layers on semi-insulating substrates showed that Cr outdiffused readily during deposition, approaching a level of $(1\text{-}2)\times10^{16}$ atoms cm^{-3} throughout the epitaxial layer. After deposition of a 1000 Å-thick Au film on the LPE layer and annealing at 350°C for variable times, we observed essentially the same redistribution of Cr at the near surface region and within the Au film as shown in Figure 27.

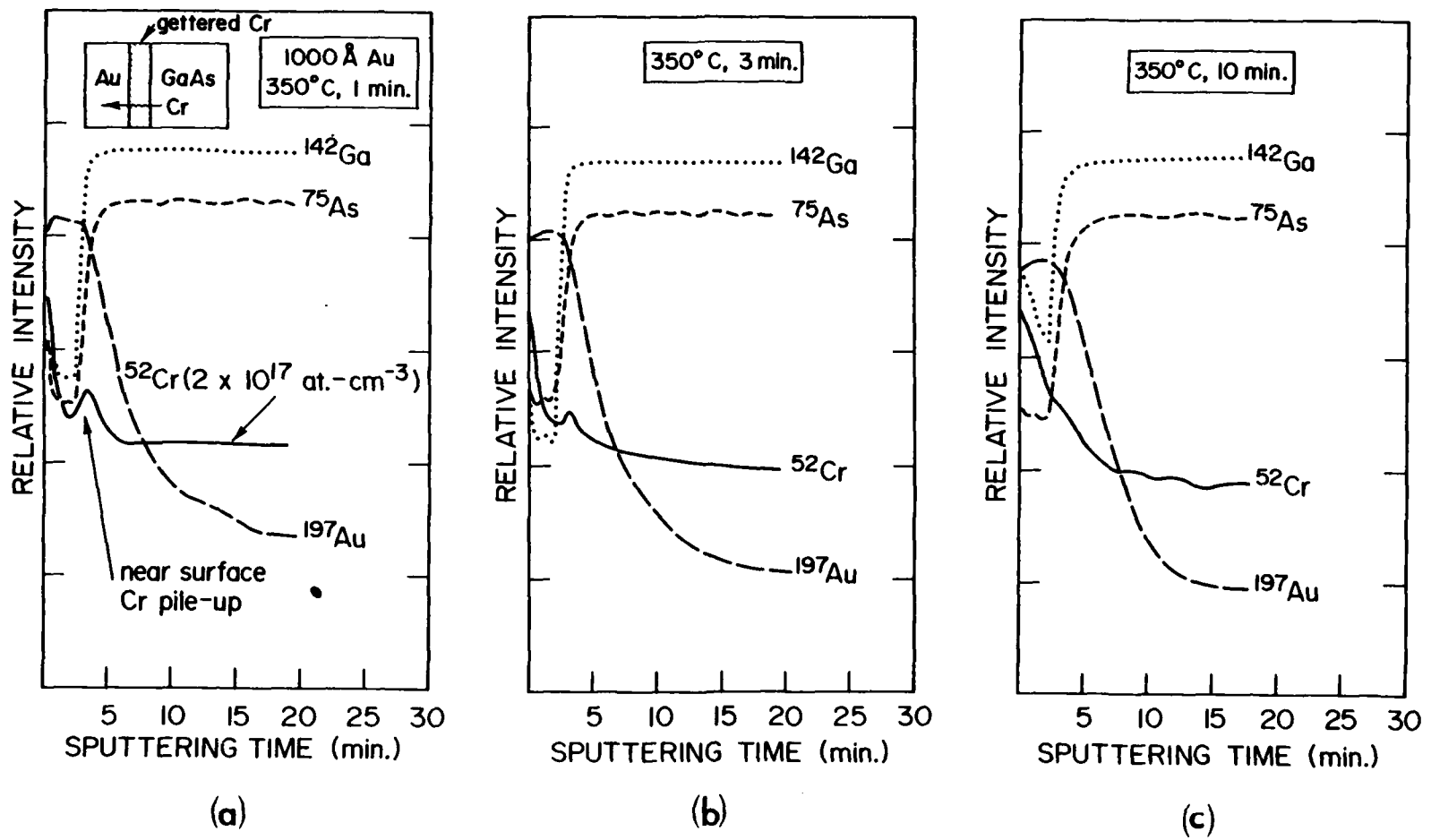


FIGURE 27. SIMS PROFILES OF (1000 Å) Au/GaAs STRUCTURE AFTER ANNEALING AT 350°C; a) t_A = 1 min; b) t_A = 3 min; c) t_A = 10 min.

To further investigate the effect of alloying on the redistribution of Cr, we increased the thickness of Au films on semi-insulating substrates to 4000Å annealed at 350°C for periods of 1 to 10 min. Figure 28 shows the resulting SIMS profiles of the Au/GaAs structure after anneals of 1 to 10 min. Qualitatively, we observe a similar pattern of Cr outdiffusion and gettering within the near-surface region, producing a sharply defined "knee" in the Cr-concentration profile after a 1-min anneal (Figure 28a).

From the data shown, we can conclude that alloying of Au films on semi-insulating GaAs substrates or LPE layers on (semi-insulating) GaAs produces a region of damage and strain within the GaAs lattice. The concentration of damage increases as a function of initial film thickness for comparable anneal durations at 350°C. This induced damage can serve as an effective gettering region for Cr (and potentially other impurities).

In all cases, Cr outdiffuses readily into the Au layer at 350°C and accumulates at the surface of the film. The data suggest that the degradation or aging of Au-Ge or Au-Ge-Ni contacts on n-type epitaxial layers grown on semi-insulating (Cr-doped) GaAs wafers may be related both to the generation of dislocation lines and the outdiffusion and gettering of Cr at the contact region.

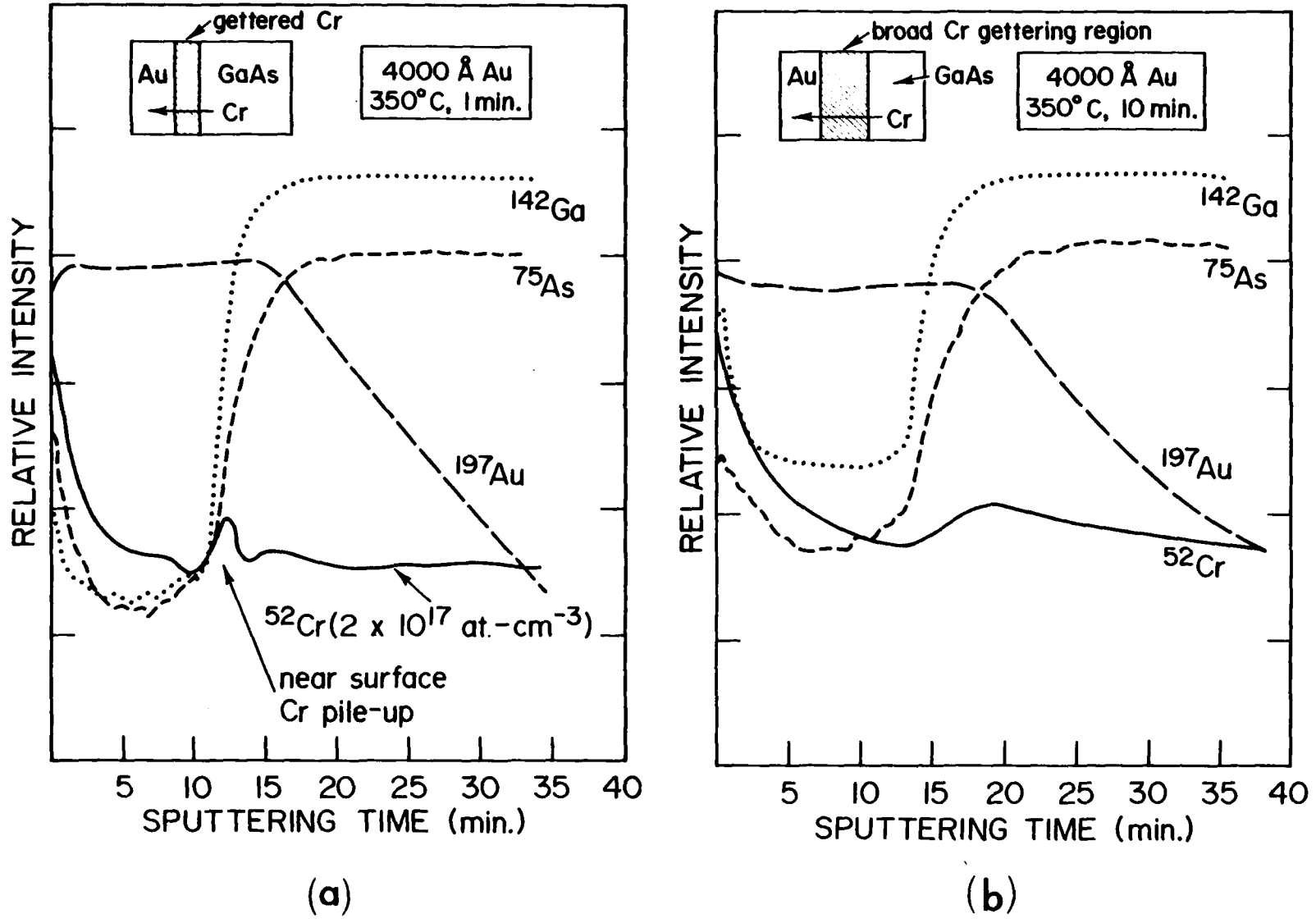


FIGURE 28. SIMS PROFILES OF (4000Å) Au/GaAs STRUCTURE AFTER ANNEALING AT 350°C; a) t_A=1 min; b) t_A=10 min.

10. PERFORMANCE OF FET STRUCTURES FABRICATED IN VPE LAYERS ON PRE-GETTERED SUBSTRATES

In the previous section, it was shown that significantly improved VPE layers are obtained when the epitaxial structures are grown on pre-gettered SI-GaAs substrates. In addition to reducing the substrate defect density at the front surface and within the interfacial region, back-surface-defect pre-gettering techniques were found to significantly reduce the outdiffusion and redistribution of Cr during deposition and subseqeunt annealing. To ascertain the effectiveness of these techniques for improving the yield and performance of FET devices, it was necessary to evaluate the interface mobility, capacitance and actual performance of FETs fabricated in VPE layers on pre-gettered substrates.

Samples used in this experiment were selected at random from wafer lots with no pre-screening tests performed, thereby assuring that the wafers were representative of as-recieved material from the supplier. One half of selected wafers was used for control specimens and the other half used for gettering and VPE layer growth. Pre-gettering was accomplished using techniques described in the previous sections and earlier reports. A getter pre-anneal was done at 800^{o}C for 30 minutes on back-surface-damaged samples with a plasma-deposited (low-oxygen-content) Si_3N_4 cap on the front surface. After annealing and removing the Si_3N_4 cap, VPE layers were grown on the substrates in a standard hydride reactor at Avantek, Inc.

Figures 29 and 30 show representative data obtained at Avantek on VPE layers grown on control (not gettered) and pre-gettered Cr-doped substrates. It is apparent that the mobility at the interface on the pre-gettered sample is significantly higher than that observed on the control sample. Tables 1 and 2 present representative comparative data obtained at 6 GHz, 12 GHz, and 18 GHz on FET devices fabricated on control and pre-gettered wafers. The data sheets illustrate the improvement of FETs in epi-layers on pre-gettered substrates. Of particular significance is the reduction (0.7 dB) in noise figure at 18 GHz.

The results show that pre-gettering of GaAs substrates yields the following:

- o Reduction or annihilation of defects within the substrate and epitaxial layer.
- o Reduction of Cr outdiffusion from the substrate during deposition and subsequent annealing.
- o Higher interface mobilities.
- o Lower noise figure at high frequencies.
- o Lower input capacitance.
- o Higher apparent device yields per wafer.

To provide further verification of the use of pre-gettering as a processing step, we then conducted a standard production run on 10 wafers selected at random from in-coming lots and FET's were manufactured on VPE layers on pre-gettered substrates. Evaluation of devices manufactured on these substrates showed similar improvements and the results were consistent with the previous data. Improvements in device yields were noted in the range of 30 to 50 percent relative to control wafers on a number of substrates.

FIGURE 29. PROFILE-VPE/GaAs (CONTROL) SAMPLE.

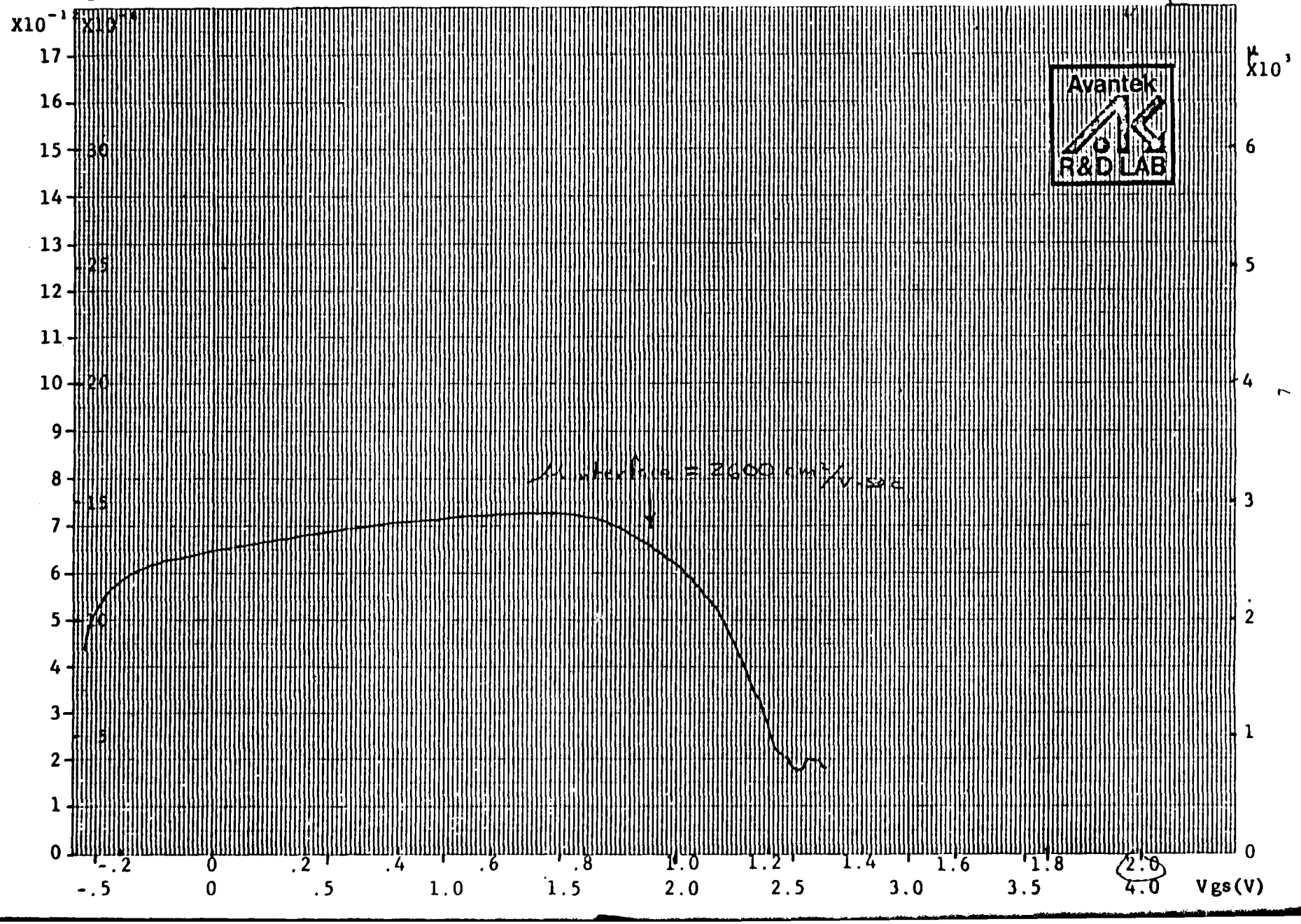
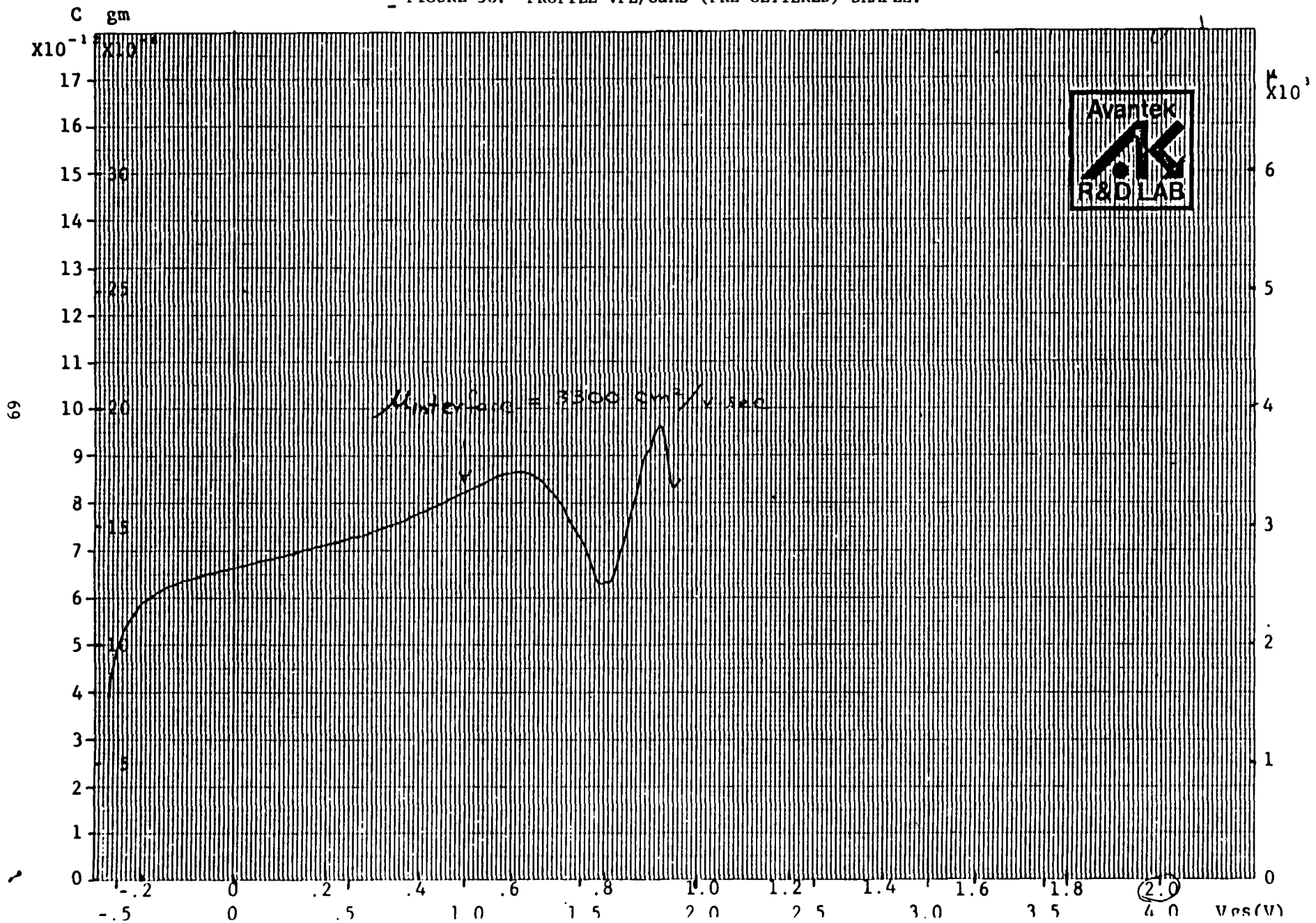


FIGURE 30. PROFILE-VPE/GaAs (PRE-GETTERED) SAMPLE.



	Test		1	2	3	4	5	6	7	8	9	10
DC	I_{dss} at V_{ds} 3 V		45	46	31	29	30					
	R_{do}		16	16	20	21	20					
	G_{mo} at V_{ds} ____, I_{ds} ____											
	G_{mo} at V_{ds} =3V, I_{dss}		50	49	45	44	45					
	V_p at V_{ds} =3V, I_{ds} =1 mA		1.0	1.1	.78	.74	.78					
	BV_{gs} at I_{gs} =1(10 µA)		7.2	7.5	10	11	11					
RF	6 GHz, F_2= 2.65 dB, DATE 6/14/79	V_{ds}/I_{ds} (V/mA)	4/8	4/7	4/7	4/8	4/7					
		F_{12} (dB)	1.7	1.6	1.65	2.0	1.75					
		GA (dB)	12.2	12.3	12.2	12.1	12.4					
		F_0 (dB)	1.55	1.45	1.5	1.86	1.61					
		F_∞ (dB)	1.63	1.53	1.58	1.95	1.69					
	12 GHz, F_2= ____ dB, DATE / /	V_{ds}/I_{ds} (V/mA)	3.5/10	4.5/7	6/5	4/6	3.5/5					
		F_{12} (dB)	2.8	2.65	2.8	3	3					
		GA (dB)	9.8	9.6	8.3	8.6	8.7					
		F_0 (dB)	2.31	2.11	2.07	2.37	2.31					
		F_∞ (dB)	2.51	2.31	2.37	2.65	2.66					
	18 GHz, F_2= ____ dB, DATE / /	V_{ds}/I_{ds} (V/mA)	12/12.5	4.1/9	10/2.	7.7/6.5	10/7					
		F_{12} (dB)	4.5	3.9	4.6	4.3	4.35					
		GA (dB)	7	7.2	6.8	6.5	6.7					
		F_0 (dB)	3.21	2.68	3.28	2.74	2.90					
		F_∞ (dB)	3.79	3.26	3.85	3.29	3.44					

TABLE 1. DEVICE DATA : CONTROL (UNGETTERED) SUBSTRATE

	Test		1	2	3	4	5	6	7	8	9	10
DC	I_{dss} at V_{ds} 3 V		34	34	34	7	7.5					
	R_{do}		21	20	21	54	54					
	G_{mo} at V_{ds} ——, I_{ds} ——											
	G_{mo} at V_{ds} =3V , I_{dss}		43	42	43	25	26					
	V_p at V_{ds} =3V , I_{ds} =1 mA		1.0	1.0	1.0	.36	.36					
	BV_{gs} at I_{gs} =1(10 µA)		4.4	12	12	18	18					
RF	6 GHz, F_2= 2.65 dB, DATE 6/14/79	V_{ds}/I_{ds} (V/mA)	3/7	2.5/8	2.5/8	2/6	2/6					
		F_{12} (dB)	1.55	1.6	1.6	1.8	1.8					
		GA (dB)	12.0	12.1	12.4	12.0	11.5					
		F_0 (dB)	1.39	1.44	1.45	1.65	1.63					
		F_∞ (dB)	1.46	1.52	1.53	1.74	1.73					
	12 GHz, F_2= ____ dB, DATE / /	V_{ds}/I_{ds}(V/mA)	2.5/9	3/8	3/7	2.5/7	/					
		F_{12} (dB)	2.5	2.6	2.55	3.4						
		GA (dB)	10.1	9.6	9.8	8.8						
		F_0 (dB)	2.51	2.06	2.53	2.56						
		F_∞ (dB)	2.18	2.25	2.21	3.16						
	18 GHz, F_2= ____ dB, DATE / /	V_{ds}/I_{ds} (V/mA)	6/9	6.5/6	6.2/9.5	5.3/3.5	/					
		F_{12} (dB)	3.8	3.15	4.10	4.70						
		GA (dB)	7.7	6.3	7.3	5.45						
		F_0 (dB)	2.51	2.13	2.57	2.83						
		F_∞ (dB)	2.89	2.62	3.6	3.37						

TABLE 2. DEVICE DATA : PRE-GETTERED SUBSTRATE

11. LOW-TEMPERATURE GETTERING OF Cr IN GaAs

A number of recent investigations have shown that Cr in semi-insulating GaAs can be rapidly redistributed at annealing temperatures in the range of 750-1000°C. This occurs at the front surfaces of GaAs samples as the result of stress induced by an encapsulant layer,[45,46] within ion-implanted regions,[46-48] or at back-surface-damage zones[24,27,42] produced by mechanical abrasion or ion implantation.

Efficient gettering of mobile Cr and the reduction of its presence in front-surface defect zones has been shown to be attainable in GaAs wafers when rotary abrasive back-surface mechanical-damage techniques are employed.[24,27] Stress-field gradients introduced by the laterally continuous dislocation line array at the backside are responsible for the observed gettering behavior. Such gettering has been shown to be extremely effective at normal processing temperatures when the maximum annealing time is <4 hr.

In our previous investigations of Cr gettering by back-surface damage, annealing temperatures exceeding 650°C have largely been utilized. However, recent studies have shown that Cr can be gettered at 350°C during alloying of Au films on GaAs.[49] Strain effects at the interface and Au indiffusion are thought to be responsible fo the redistribution and gettering of Cr into regions of near-surface alloy damage. These results suggested that Cr might be gettered from bulk GaAs wafer by back-surface damage at temperatures as low as 300°C. In this section,we present data from secondary ion mass spectrometry (SIMS) measurements on back-surface mechanically damaged wafers showing the low-temperature gettering of Cr in GaAs.

Chromium-doped GaAs wafers used in this study were of (100) orientation with resistivies $>10^7$ Ω-cm. Using a recently developed rotary abrasive technqiue described in earlier reports,[5-9] concentric damage grooves (<60 μm in depth) were produced at the back surfaces of wafers. An SiO_2 film was deposited on the front surface in a commercial pyrolitic reactor at 400°C as a scratch protection layer during rotary abrasion of the wafer backside. Upon completion of the damage process, the SiO_2 films were removed and samples subsequently cleaned and dried. Annealing was done in flowing H_2 at temperatures in the range 300-400°C, for periods of 10-300 h. Chemical in-depth profiling was performed on the GaAs back surfaces in a Cameca IMS-3f ion microanalyzer, using O_2 bombardment combined with positive secondary ion mass spectrometry. To provide a quantitative measure of the gettered-Cr concentration, a ^{52}Cr ion implant into GaAs was used as a calibration standard.

Transmission electron microscopic examination of back-surface-damaged wafers showed that a continuous array of nested dislocations, extending to a depth of $\underline{\sim}1.5$ μm below the depth of damage grooves, was produced by the rotary abrasive process, in agreement with previous results. After annealing for 300 h at 350° and 400°C, we observed no significant alteration in dislocation line density or lateral/vertical distribution at the back surface.

In Figure 31, we show a plot of the measured dislocation line density as a function of depth (below damage grooves) from the back surface. Also shown are the relative ^{52}Cr ion intensity profiles obtained at the back surface after damage introduction (no anneal) and after annealing at 350°C for 65 and 274 h. After a 65-h thermal annealing, the Cr is concentrated with a region $\underline{\sim}0.75$ μm below damage grooves at the back surface. After 274 h of annealing the Cr is gettered throughout the damage region, yielding a graded distribution that is indicative of the

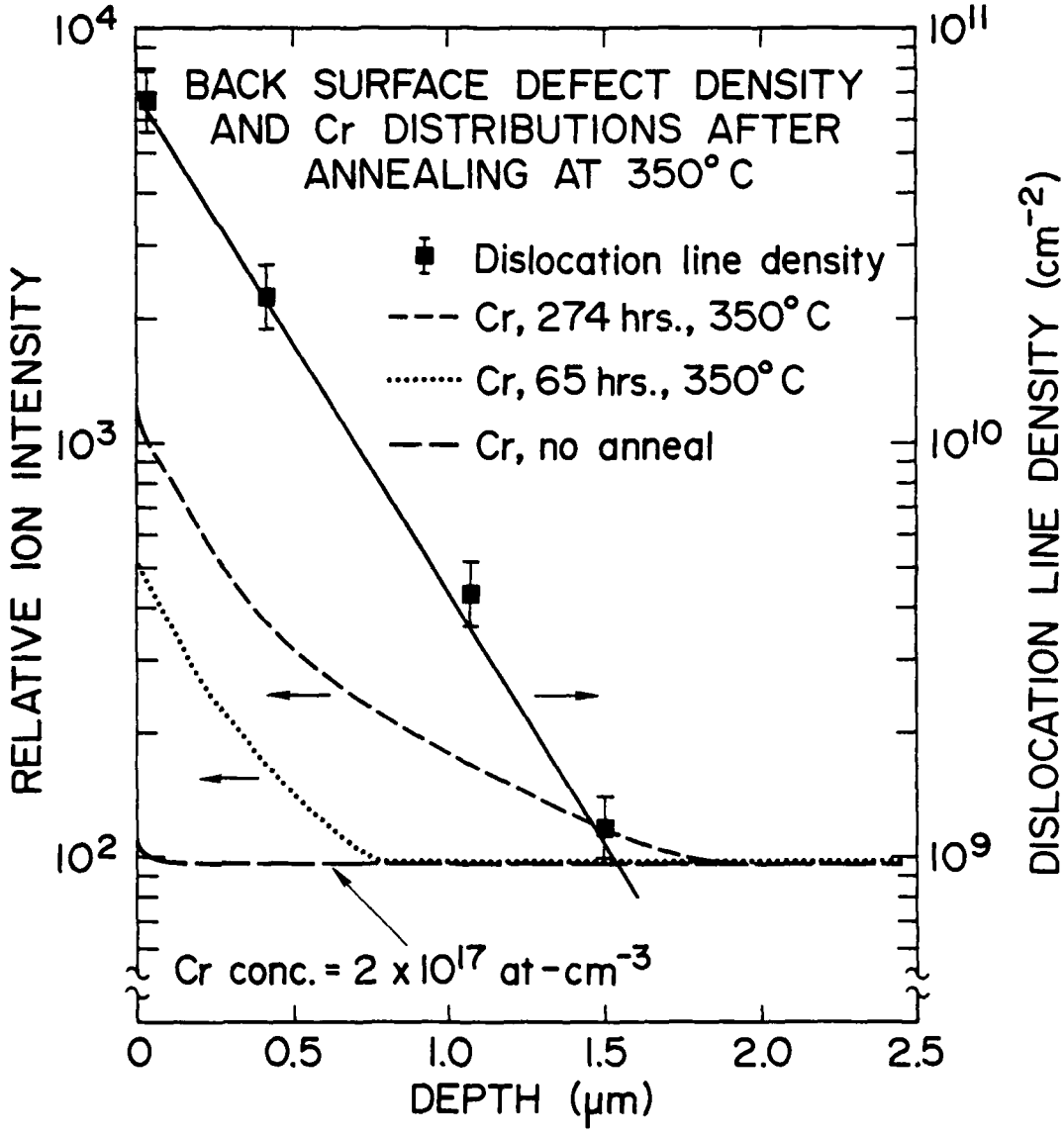


FIGURE 31. BACK-SURFACE DEFECT CONCENTRATIONS AND GETTERED Cr DISTRIBUTIONS AFTER 350°C ANNEALING.

decreasing dislocation line density with increasing depth from the back surface. We detected a similar increase in the amount of gettered Cr as a function of annealing time at temperatures of 300 and 400°C. These experiments were repeated on a number of samples damaged and annealed under the same conditions with essentially identical results. In all cases,we were unable to detect any evidence of "reverse" (degetter) annealing[42] as the anneal time was increased. These results are in agreement with the TEM data, which showed no significant loss of dislocation line structure as a function of increasing annealing time at low temperatures.

In Figure 32,we show the gettered-Cr content obtained by integrating the Cr concentration profiles over the gettering depth (from the back surface) for various anneal times at temperatures between 300 and 400°C. The baseline for integration was set at the background (bulk) Cr doping concentration ($2x10^{17}/cm^3$) and was the same for all samples used in these experiments. The limit of integration was set at the point where the gettered-Cr profile intersected the baseline or background Cr doping level.

Of particular significance in Figure 32 is the fact that the amount of gettered Cr increases exponentially as a function of $t^{1/2}$ at each of the annealing temperatures. The semilog plot of gettered-Cr concentration versus $t^{1/2}$ at each of the temperatures yields straight-line plots that are parallel and intercept the vertical axis at nonzero values of Cr concentrations when the lines are extrapolated to t = 0. Two possibilities are suggested for this apparent concentration of Cr at t = 0: either Cr is always present in negligibly small quantities at the surface after mechanical abrasion, or during the initial period of low-temperature annealing a rapid motion and gettering of Cr occurs, independent of any surface concentration introduced by the abrasion process.

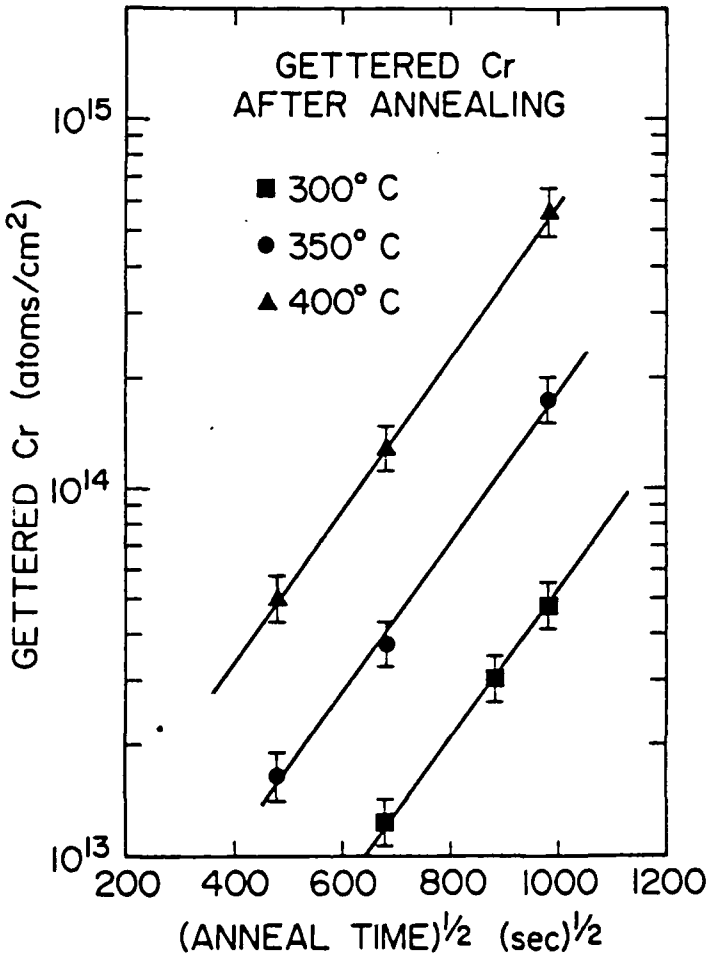


FIGURE 32. GETTERED Cr CONCENTRATIONS AFTER ANNEALING AS A FUNCTION OF $t^{\frac{1}{2}}$.

Our data show that the former is the more likely possibility. However, in either case, the SIMS process does not permit an adequate resolution of the low (gettered) Cr concentrations superimposed on the high bulk background at these temperatures for annealing times less than 20 h.

To further investigate the gettering behavior, we have plotted the amount of gettered Cr as a function of $10^3/T(K)$ for two annealing times as shown in Figure 33. The activation energy was calculated to be 0.88 $\pm$ .06 eV.

The data obtained suggest that the amount of gettered Cr, (atoms/cm^2), can be described by an equation of the form,

$$\phi = C_o \exp(-E/kT)\exp(\theta t^{1/2}), \qquad (1)$$

where C_o and θ are constants, E is the activation energy, k is Boltzmann's constant, and T is the annealing temperature. If indeed valid, the amount of gettered Cr should be predictable at any temperature or annealing period, provided the thermal (damage) stability limit has not been exceeded, i.e., reverse annealing is absent. Using values for the constants C_o and θ determined from the experimental data of Figures 32 and 33, we calculated the amount of gettered Cr expected for 750 and 800°C thermal treatments for times of 1/2 and 1 h. Back-surface damage was then introduced into wafers containing the same background Cr doping level as the samples used in the low-temperature gettering experiments and rotary abrasion conditions controlled to produce approximately the same back-surface defect concentrations. Annealing was subsequently done in flowing H_2 at 750 and 800°C for periods of 1/2 - 1 h. In each case, we correlated the experimentally determined and predicted amounts of gettered Cr at the back surfaces and found extremely good agreement ($\pm$ 10%), verifying the

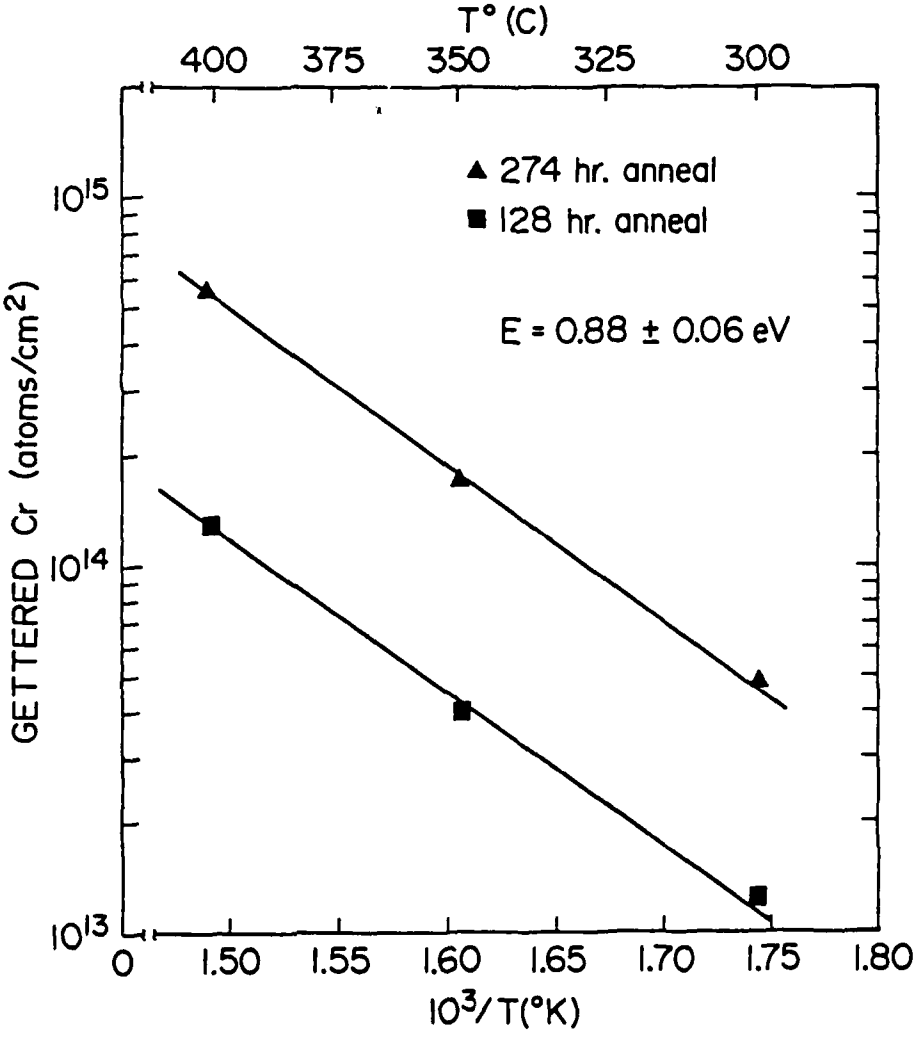


FIGURE 33. BACK SURFACE GETTERED Cr CONCENTRATION VERSUS RECIPROCAL TEMPERATURE FOR 128 HOUR AND 274 HOUR ANNEALING PERIODS.

applicability of Eq. (1) in describing Cr gettering behavior in heavily damaged regions at temperatures and annealing periods below the point at which dislocation annihilation occurs.

The flux of Cr atoms moving into the damage regions can, in the simplest form, be described by[50]: $\bar{J} = (DC/kT)\bar{F}$, where $\bar{F}$ is the net force exerted on the C atom in the presence of a large stress field, C is the Cr concentration, and D is the diffusion coefficient. The magnitude of $\bar{F}$ will be determined by the level of damage, and consequently the flux and total number of gettered atoms should depend on the dislocation line density and stress gradient produced at the back surface.

To provide a qualitative comparison of the effect of varying damage levels on the Cr gettering efficiency at low temperatures, we prepared two samples from the same wafer with different levels of back-surface damage and annealed at 400°C for 274 h in flowing H_2. From SIMS profiles, we determined that the concentration of gettered Cr was significantly reduced in the sample containing the lower amount of damage, thereby confirming that the low-temperature gettering observed in this investigation is largely influenced by the magnitude of the driving force provided by the elastic stress gradient at the back surface.

12. INCORPORATION OF BORON DURING GROWTH OF GaAs

In addition to its classic use for microwave devices, GaAs is rapidly becoming the material of choice for high speed digital circuits. The two common materials preparation schemes for the fabrication of such devices involve the use of epitaxial layers grown on semi-insulating GaAs wafers or direct ion implantation and annealing of bulk insulating substrates.

The latter method would appear to be straight forward process. However, many problems have been encountered due to the unpredictable behavior of ion-implanted GaAs. These problems include the irreconcilable difference between the atomic profiles in the implanted material and the resultant electrical carrier concentrations; the occasional greater than 100% electrical activation after post-implant annealing; and type conversion of intentionally encapsulated and annealed material with no additional donor atoms being introduced. Many of the problems associated with processing can be attributed to Cr redistribution[42,45-47,51] during the thermal annealing. Unless intentional doping is employed, the conventional Bridgman or gradient freeze techniques employed for GaAs growth, generally yield n-type material, due to the incorporation of residual donor impurities. Chromimum is intentionally added during growth to compensate these residual donors and to raise the resistivity of the material to the levels necessary for the production of devices in this near-surface region. Recent studies have shown that the encapsulation and annealing processes can change the Cr in-depth distribution. This change in Cr distribution can electrically activate previously compensated donors, causing conversion of the material and the addition of these released donors to the intentional donors added to the material by ion implantation. Although these results have not solved the problems associated with Cr redistribution, the increased level of understanding has provided a clearer basis for future solutions in GaAs processing.

Several research groups have developed the use of liquid encapsulated Czochralski (LEC) growth methods to reduce the residual donor level and, thereby, produce semi-insulating GaAs without the intentional addition of a Cr acceptor. These groups use either pyroltyic boron nitride (pBN) or quartz as the crucible material for growth and encapsulate both the growing crystal and the melt in liquid boric oxide.[52,53]

As with any technique, one must be concerned with the incorporation of impurities during crystal growth, particularly boron from this boron rich growth system. Should boron be incorporated during the growth process and, moreover, exhibit some electrical behavior, it is important to assess the magnitude of the incorporation and resultant role of the impurity insofar as it influences the electrical characteristics of the growth material. Rao, Duhamel, Favennec and L'Haridon[54] have discussed the possibility of B being a deep-level acceptor in GaAs. Thus, its presence might compensate residual donor impurities and one is therefore faced with a variety of questions:

1. Is B incorporated during LEC growth of GaAs and from the boat or the encapsulating liquid source?

2. If semi-insulating material results from this growth, is it because the growth processes are truly cleaner than in the case of Bridgman growth techniques, or is it because B is incorporated accidentally during growth and is causing compensation of any residual donors contained in the material?

3. If B is being incorporated and acting as an acceptor similar to Cr in Bridgman-type material, does B redistribute under thermal processing as has been found for Cr?

The purpose of this investigation was thus two fold: First, to provide an assessment of the incorporation of B into GaAs grown by the liquid encapsulated Czochralski methods and, secondly, to investigate the redistribution of B upon thermal processing. These analyses were performed using a CAMECA IMS-3f Ion Microanalyzer with oxygen-ion bombardment. This mode of operation provided detection limits for Cr and B in the range 10^{13} to 10^{15} atoms per cubic centimeter. To evaluate the relative contributions of the starting materials, the pBN crucible and the boric oxide encapsulant, we obtained 28 different pieces of single-crystal GaAs from 11 separate growers. These were grown by the Bridgman or gradient freeze technique, by the LEC method in quartz, or by the LEC method in pBN. These materials were analyzed on several different days with the observed ion intensities converted to atomic densities using a known boron ion implant in GaAs.

The quantitative results are tabulated in Table 3 by growth technique. The amount of boron incorporated during conventional Bridgman growth is remarkably low and tightly clustered about the average of 6.1×10^{14} at-cm^{-3}. Since these values represent material from four different laboratories, one can surmise that the respective sources of Ga and As do not contain significantly variable amounts of boron. The corresponding analyses of the LEC quartz-grown material shows a small, but statistically significant, increase in the boron content. Again, there is a tight clustering about the average of 1.4×10^{15} at-cm^{-3}. The small difference in the boron content of these two types of growth methods suggests that there is only a small contribution from the boric oxide encapsulant.

Table 3

BORON CONCENTRATIONS IN GaAs WAFERS

Method	Suppliers	Studied	Average B Conc ($at\text{-}cm^{-3}$)	% Relative Standard Deviation
Bridgman	4	10	$(6.1 \pm 3.7) \times 10^{14}$	61
LEC/Quartz	4	8	$(1.4 \pm .9) \times 10^{15}$	61
LEC/pBN	3	10	$(1.6 \pm 1.2) \times 10^{17}$	80

Examination of the boron data from LEC-pBN material shows at least a 100-fold increase in the boron contamination over that in the first two growth methods. This strongly supports the suggestion that there is some dissociation of the pBN crucible and consequent boron incorporation in the molten GaAs. We have no immediate explanation for the larger variation in the boron concentrations found in the pBN materials compared to those prepared by Bridgman on LEC-quartz techniques. Perhaps these variations result from the nuances of the growth techniques from laboratory to laboratory.

Having found concentrations of boron at "doping levels" in the LEC material, it is appropriate to examine the boron mobility under thermal processing. To this end, we implanted ^{11}B at 100 keV to a dose of 5×10^{14} B/cm^2 into conventional Cr-doped semi-insulating GaAs. A section of the as-implanted material was set aside as a control sample and the remainder encapsulated with Si_3N_4 and annealed for 30 minutes at 850°C. The encapsulant was removed and both pieces of material were analyzed by SIMS to determine the ^{11}B in-depth distribution. Figure 34 shows the as-implanted and annealed profiles. No movement of the boron could be detected at these processing conditions, suggesting that the boron diffusion coefficient in GaAs is less than 1×10^{-14} cm^2 - sec^{-1} at 850°C. However, the Cr redistribution resulting from these conditions is clearly evident from the Cr depletion indicated in Figure 34.

This study shows that significant amounts of boron are incorporated during LEC growth and that the incorporated boron is not mobile at normal processing temperatures. Thus, it becomes of both scientific and technological importance to determine in future studies if boron is indeed a deep-level acceptor in GaAs or merely an electrically neutral impurity.

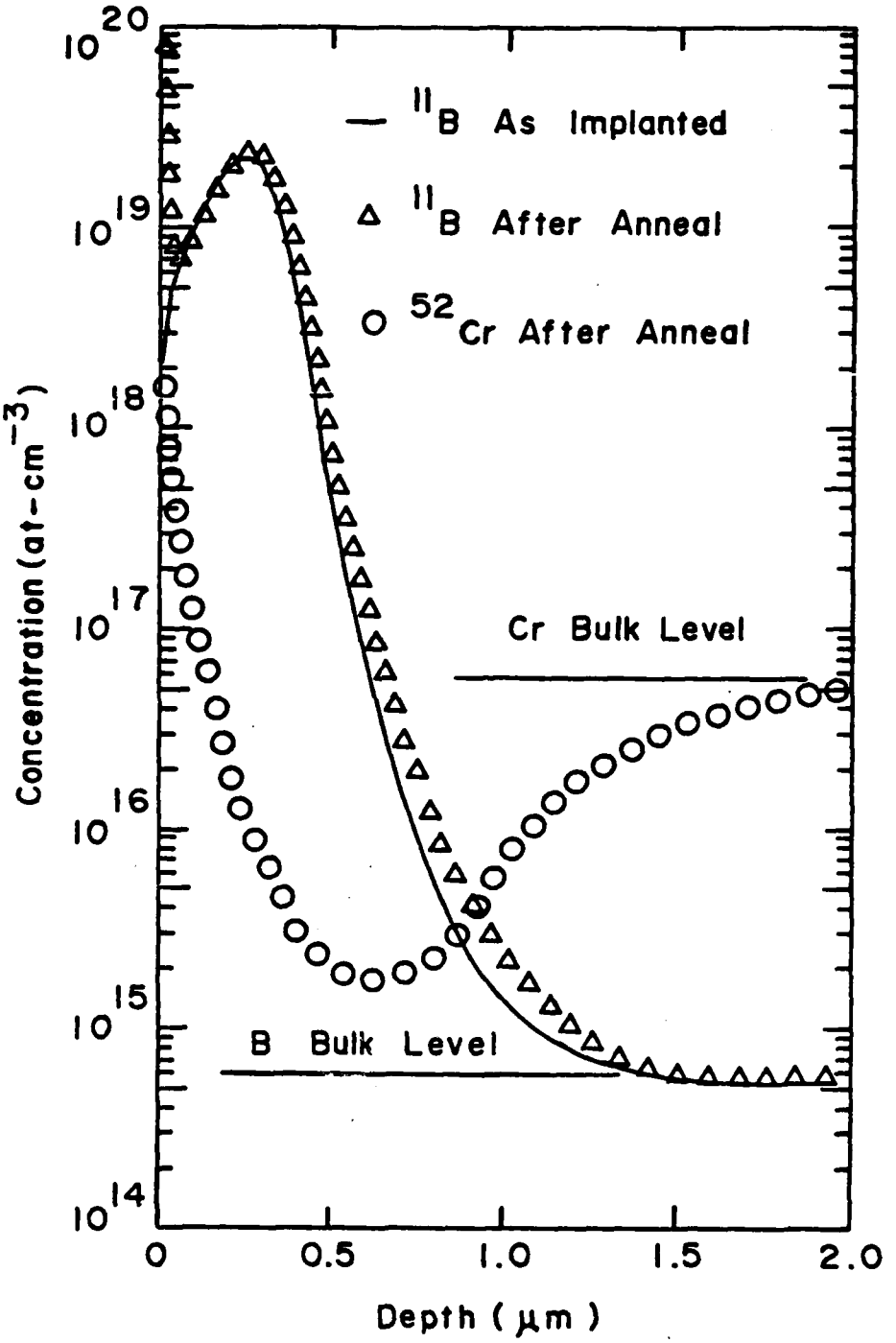


FIGURE 34. BORON AND CHROMIUM DISTRIBUTIONS IN BORON-IMPLANTED GaAs AFTER ANNEALING AT 850°C.

13. LOW TEMPERATURE REDISTRIBUTION OF Cr IN BORON-IMPLANTED GaAs IN THE ABSENCE OF ENCAPSULANT STRESS

Recent investigations have shown that Cr is rapidly redistributed in GaAs at annealing temperatures in the range, 300°C to 1000°.[27,42,45-49,55] It has been suggested that the presence of an encapsulating layer on the surface of GaAs introduces significant stress at the interface, resulting in Cr motion toward the surface and depletion of Cr in the underlying material.[45-47] In the case of ion implanted and annealed GaAs, both the encapsulant and residual damage retained in the sample contribute to the diffusion of Cr into the surface region. At the present time, however, there have been no published reports which separate the roles of ion-implantation damage and encapsulant on Cr diffusion and gettering.

In this section, we present data on the motion of Cr into regions of implantation damage at temperatures in the range of 300°C to 600°C in the absence of a surface encapsulating layer.

Gallium arsenide wafers used in this investigation were of (100) orientation ($\pm 3^{o}$) and Cr doped to obtain resistivities $>10^{7}$ μ-cm. After cleaning, the semi-insulating wafers were implanted with 100-keV B ions to doses in the range of 1×10^{14} ions cm^{-2} to 1×10^{15} ions cm^{-2}. A boron implant was chosen for this study because of its relatively low diffusivity in GaAs at temperatures as high as 850°C,[56] thus enabling the implant profile to serve as an effective depth scale reference marker. Since the purpose of this study was to isolate and investigate the role of damage in the redistribution of Cr, we have chosen to thermally process the GaAs at temperatures below 600°C in flowing H_2.

Following implantation and/or annealing, samples were cut into 3 mm x 3 mm squares. Specimens for transmission electron microscopy/diffraction (TEM/TED) analysis were prepared by conventional jet thinning techniques and examined in the microscope. Secondary ion mass spectrometry (SIMS) profiling was performed on similar samples using a Cameca IMS-3f ion microanalyzer with O_2 primary ion bombardment and positive secondary ion spectroscopy. Both the Cr and B atomic concentrations were calibrated using standards prepared by ion implantation of $^{52}Cr^+$ and $^{11}B^+$ into GaAs substrates.

The TEM examination of unannealed, implanted samples indicated that microstructural defects were below the resolution limit and selected area TED analysis indicated that the single-crystal structure was retained at all dose levels investigated. After annealing at 300°C for varying periods, we were unable to clearly resolve any identifiable damage within the ion-implanted regions. However, after annealing at 400°C for 20 hrs., we detected the presence of dislocation loops of an average (image) diameter of 50 Å. The maximum concentration of loops was $<10^{10}$ cm^{-2}, with the density increasing as a function of implant dose. In samples implanted and annealed at 500°C, we detected loops of similar average size and a concentration of 10^{11} cm^{-2}. In all specimens examined, we observed the nucleation of small dislocation loops of an average size of 50 Å, increasing in concentration as a function of increasing annealing temperature and duration.

For correlated data on the motion of Cr in implanted and annealed samples, we obtained SIMS profiles of the Cr concentration as a function of depth from the surface. In Figure 35, we show profiles of the B and Cr concentration in GaAs samples implanted with $^{11}B^+$ to a dose of 10^{15} ions/cm^2 and subsequently annealed in flowing H_2 at 400°C for variable periods. In Figure 35a), we

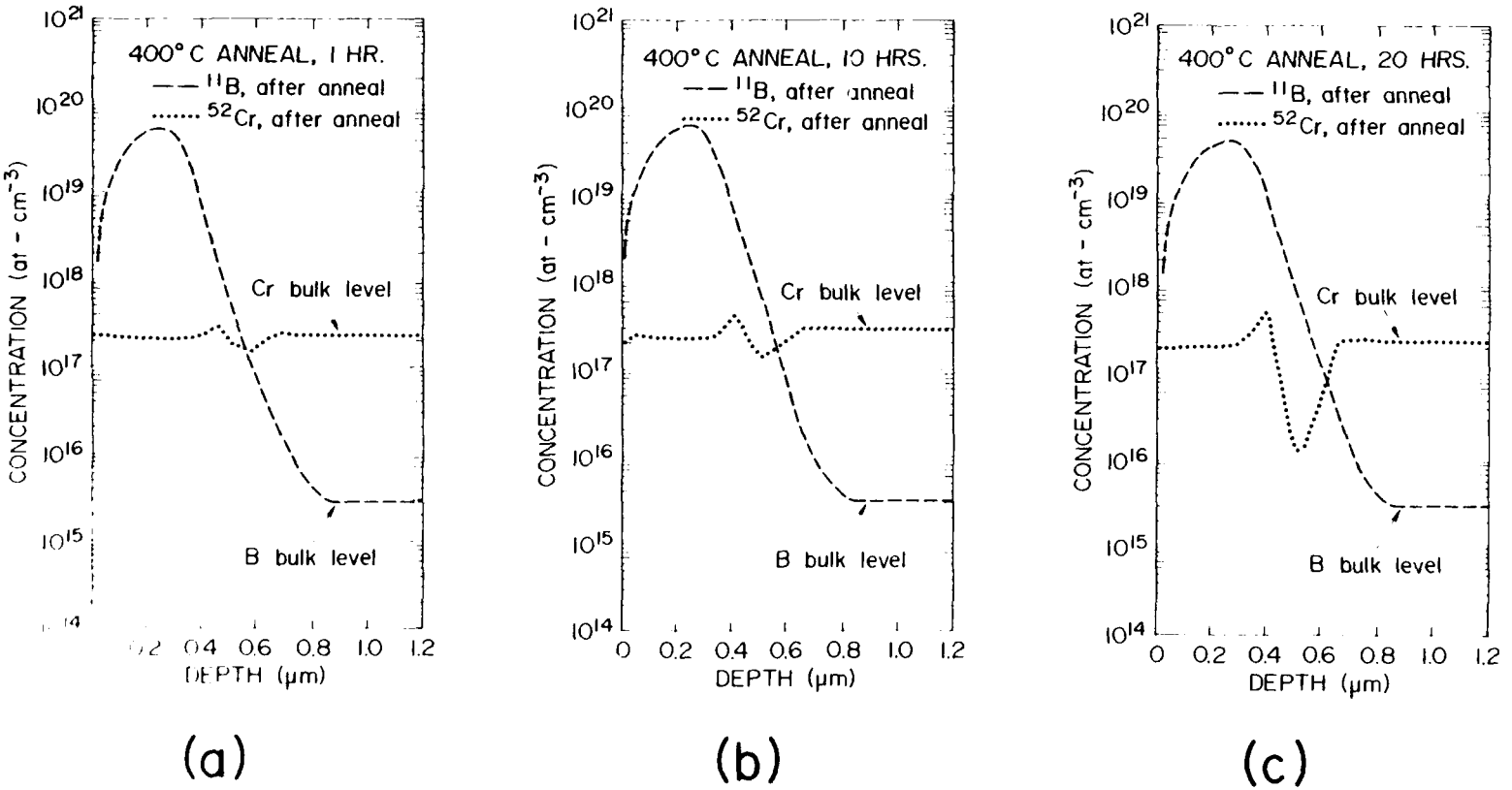


FIG 35. SIMS PROFILES OF B AND Cr DISTRIBUTIONS IN 100 keV B-IMPLANTED GaAs AFTER ANNEALING AT 400°C; a) 1 hr.; b) 10 hrs.; c) 20 hrs.

observe a slight depletion of Cr at a depth of 5100 Å after 1 hour of annealing accompanied by an apparent gettering or pileup in the adjacent region (3700 Å) within the B impurity distribution profile. This depletion and gettering is more readily detected after 10 hrs. of annealing (Figure 35b). After 20 hours of annealing at 400°C, a sharply defined depletion and gettering region is observed (Figure 35c)). In all cases, we detected no significant near-surface pileup or outdiffusion of Cr in samples annealed at 400°C.

In contrast to the results obtained at 400°C, samples annealed at 500°C exhibited rapid development of a zone depleted in Cr and subsequent gettering of Cr within damage regions. In Figure 36a), after 1 hr, of annealing, the Cr depletes to a level of $\sim 2 \times 10^{15}$ atoms/cm^3 at 5100 Å and a Cr gettering peak develops in a region at $\sim R_p$ (2550 Å) for samples implanted to a dose of 1×10^{15} ion/cm^2. At doses of 5×10^{14} ions/cm^2 and 1×10^{14} ions/cm^2, no significant differences in Cr gettering behavior are noted and essentially identical levels of Cr depletion are detected after similar annealing. After 4 hours of annealing, gettered Cr is retained within the damage regions, but some apparent movement of Cr toward the surface can be observed (Figure 36b)). This near-surface pileup of Cr is thought to be related to a stoichiometric breakdown of the GaAs surface after extended annealing at 500°C. Similar gettering of Cr within implantation damage zones and subsequent motion to the surface was also observed after a 10 hr. anneal (Figure 36c)).

In a recent study[55], we reported on low-temperature Cr motion in samples containing extensive back surface-damage produced by mechanical abrasion. In the present study, Cr is also seen to move at low temperatures in the presence of damage from a non-amorphizing ion implant. The short-range, sharply-defined Cr

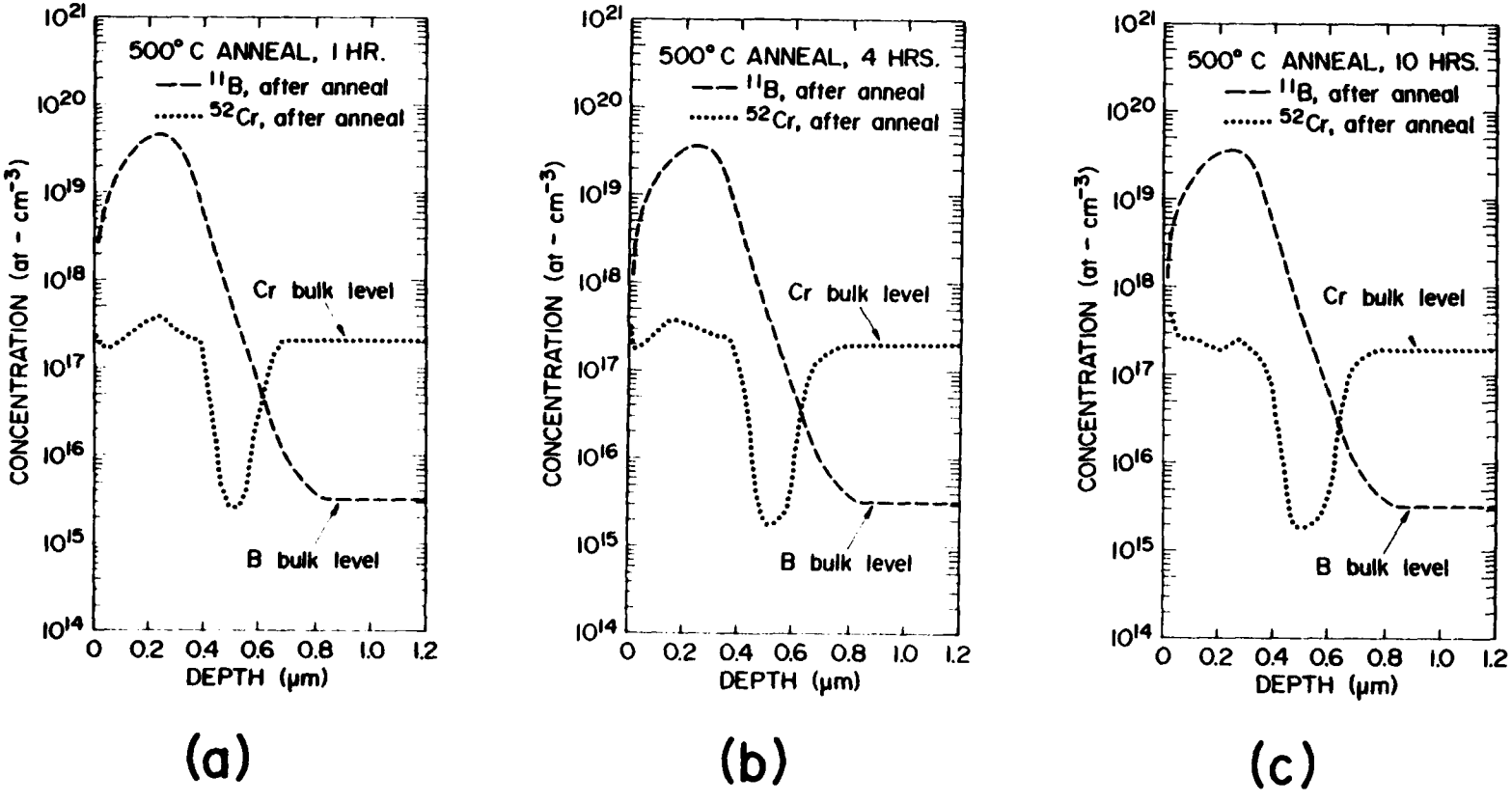


FIGURE 36. SIMS PROFILES OF B AND Cr DISTRIBUTIONS IN 100 keV B-IMPLANTED GaAs AFTER ANNEALING AT 500°C; a) 1 hr., b) 4 hrs.; c) 10 hrs.

an encapsulating layer. The exact nature of the driving force for Cr redistribution under these conditions cannot be determined. A possible explanation is that a short-range stress field mobilizes the Cr toward the implanted region. Once the Cr atoms reach the implanted region containing lattice damage and boron atoms, the Cr diffusion coefficient is reduced, causing a pile up at depths greater than R_p. Upon extended annealing at temperatures approaching 600°C, surface stoichiometric breakdown introduces an additional driving force that moves the Cr atoms closer to the surface through the implanted region.

14. ANNEALING OF DAMAGE AND REDISTRIBUTION OF Cr IN BORON-IMPLANTED Si_3N_4-CAPPED GaAs

A number of investigators have reported the redistribution of chromium in GaAs after annealing at temperatures sufficient to reorder implantation damage and electrically activate the implanted atoms.[45-48,51] When the anneal is performmed with a surface encapsulant such as Si_3N_4 or SiO_2, the details of the Cr depletion profile are related to the temperature-time parameters of the anneal, but the depleted region can extend in depth over several micrometers. The depleted chromium has been found to accumulate in the encapsulant-substrate interface and/or within zones of residual damage (in the case of ion-implanted GaAs).

The driving force for the Cr motion has been thought to be dominated by the stress field associated with the thermal expansion mismatch between the encapsulant and the substrate. A recent study of Cr redistribution in boron-implanted GaAs, annealed at temperatures between 300 and 600°C in the absence of an encapsulant, suggests that implantation damage alone can induce significant Cr motion and Cr gettering into the implanted region.[57] The Cr redistribution profiles in these cases are significantly different and easily distinguishable from those observed from processing at high temperatures in the presence of an encapsulant.

One unresolved question from these previous studies is the relative importance and role of implantation damage versus encapsulant stress on Cr redistribution over a range of annealing temperatures. Here, we present transmission electron microscopy/diffraction (TEM/TED) and secondary ion mass spectrometry (SIMS) depth profiling results which demonstrate the correlation between implantation damage annealing and Cr redistribution in B implanted GaAs annealed with a Si_3N_4 surface encapsulant. The implantation damage effect has been isolated from the encapsulant stress

effect by comparing the Cr profiles to those which can be attributed solely to implantation damage.

Samples used for this study wre prepared from <100>, Cr-doped, semi-insulating GaAs wafers with resistivities $>10^7$ Ω-cm. After cleaning, specimens were implanted with 100 keV $^{11}B^+$ to a dose of 5×10^{14} cm^{-2}. The implanted surface was subsequently encapsulated with $\sim$1000 Å of plasma deposited Si_3N_4. One hour isochronal anneals were performed on various samples in flowing H_2 at temperatures between 500 and 900°C in 50°C increments.

After removing the encapsulant layers, the implanted and annealed wafer were cut into 3 mm x 3 mm squares for TEM/TED or SIMS analysis. Samples for the TEM/TED investigation were prepared from these squares by conventional jet thinning techniques and examined using bright-and dark-field electron microscopy. A Cameca IMS-3f ion microanalyzer, with O_2 primary ion bombardment was used in obtaining Cr and B in-depth profiles. Atomic concentrations of Cr and B were determined from secondary ion intensities using standards prepared by ion implantation of $^{52}Cr^+$ and $^{11}B^+$ into GaAs substrates.

Examination of implanted control (unannealed) samples indicated that microstructural defects were either absent or below the resolution limit for detection by TEM. Selected area TED also showed that the GaAs single-crystal structure was retained after implantation. In Figure 37, we show representative bright-field electron micrographs obtained on B-implanted, Si_3N_4-capped samples after annealing for 1 hr. at temperatures of 600, 700 and 800°C. The micrographs illustrate the nucleation, growth, and subsequent decomposition of implantation-induced damage, as a function of increasing annealing temperature. After annealing at 600°C for

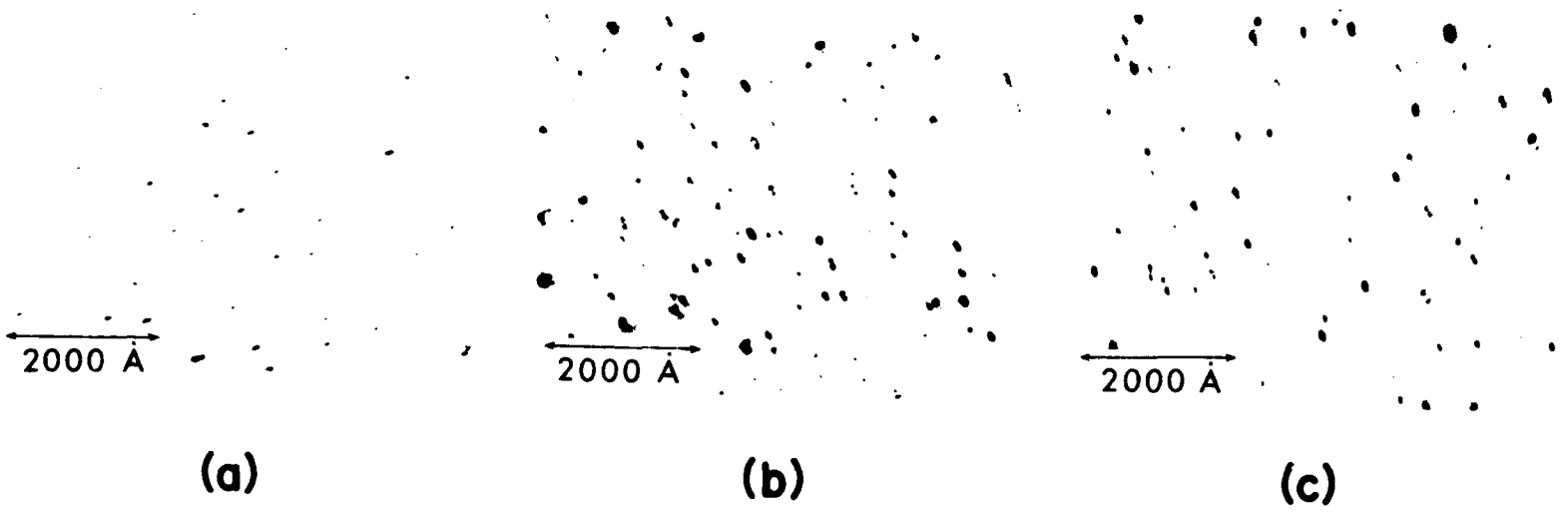


FIGURE 37. REPRESENTATIVE BRIGHT FIELD TRANSMISSION ELECTRON MICROGRAPHS OF B-IMPLANTED Si_3N_4-CAPPED GaAs SAMPLES AFTER ANNEALING; a) 600°C; b) 700°C; c) 800°C.

1 hr., we observe the presence of dislocation loops of 50-Å-diameter average (image) size. At annealing temperatures $\leq$700°C, an increase in defect density can be seen, accompanied by a corresponding increase in average dislocation loop size. In contrast, for temperatures >700°C, we observe a further increase in average defect size, but a substantial decrease in loop concentration.

Figure 38 shows a plot of the measured loop concentration and average loop (image) size as a function of annealing temperature. Of particular importance is the fact that at annealing temperatures below 700°C, we observe a phase of damage (loop) nucleation and a corresponding growth in loop size. At 800 and 900°C, the decrease in loop density indicates an annihilation of defects as a function of increasing anneal temperature. Histogram plots of the distribution of dislocation loop diameters at each temperature indicate a displacement toward larger defect sizes as the annealing temperature is increased. These data suggest that the larger loops grow at the expense of smaller defects throughout the temperature range investigated. At the higher anneal temperatures (T_A) >700°C), decomposition of dislocation loops will provide a source of defects that migrate to "sinks" or larger loops, thereby yielding an apparent increase in defect size. For $T_A \leq$700°C it is suggested that the loops increase in size by both direct interaction between smaller loops (absorption/recombination) and the attraction/binding of mobile point defects moving to existing loop sites.

To obtain information on the correlation between damage annealing and Cr redistribution, SIMS depth profiling analyses were performed on implanted samples annealed at temperatures in the range of 500 to 900°C, in 50°C increments. Figure 29 shows in-depth profiles of the B and Cr profiles after annealing for 1 hr.

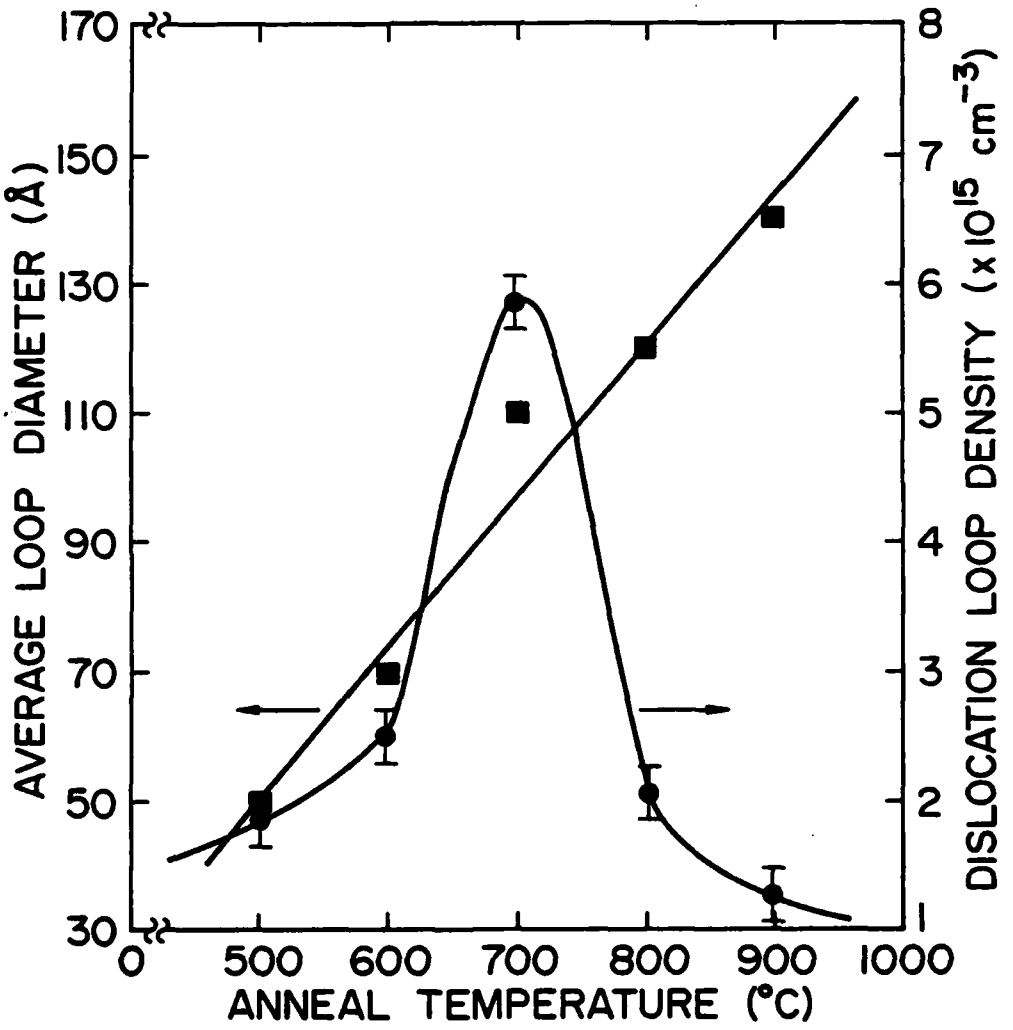


FIGURE 38. DISLOCATION LOOP CONCENTRATION AND SIZE AS A FUNCTION OF ANNEALING TEMPERATURE.

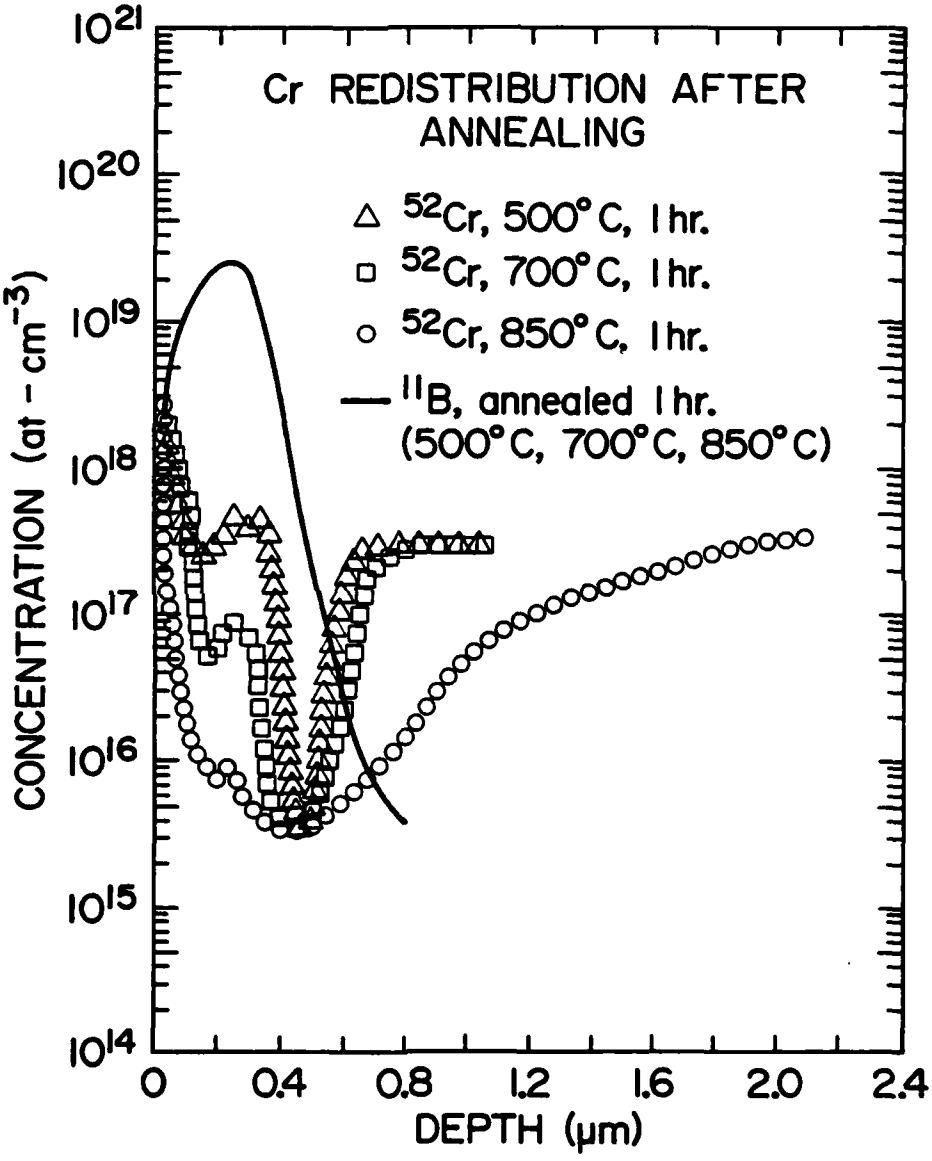


FIGURE 39. SIMS PROFILES OF Cr DISTRIBUTIONS IN B-IMPLANTED Si_3N_4-CAPPED GaAs SAMPLES AFTER ANNEALING FOR 1 HOUR AT VARIOUS TEMPERATURES.

at 500, 700 and 850°C. Essentially no diffusion or redistribtuion of the implanted B was observed at any of these temperatures, in agreement with data reported earlier. After annealing at 500°C, we observe the development of a sharply defined zone of Cr depletion at a depth of $\simeq (R_p + \Delta R_p)$ and a corresponding region of Cr gettering at R_p. In addition, a narrow near-surface region of Cr is detected. These results are in contrast to recent capless annealing results in which no near-surface Cr accumulation is detected at 500°C for 1 hr. in the absence of an encapsulating layer. The Cr distributions in the implant region are quite similar between the two annealing techniques, however, at least when annealed at 500°C.

After annealing at 700°C, we observe a pattern of Cr depletion and gettering similar to the 500°C result, accompanied by substantial motion of Cr toward the surface. The width of the Cr depletion zone is considerably increased, while the minimum depletion level remains approximately constant. The character of the Cr depletion profile is dramatically altered after annealing at 800 or 850°C. In Figure 39, we observe that Cr gettering within damage regions at R_p is reduced. Substantial motion toward the surface and outdiffusion into the encapsulant substrate interface does occur. In addition, a noticeable depletion "tail" is observed in, the substantial agreement with earlier data on ion-implanted GaAs, annealed at high temperatures and containing a surface encapsulating layer.

From the data obtained, we can conclude that the nucleation (or accumulation) of damage can be correlated with the observed Cr depletion and gettering. It is suggested that interactions between Cr atoms and dislocation loops or point defects are responsible for gettering within these damage regions. Annealing of Si_3N_4-capped samples at 500°C produces a pattern of Cr depletion and gettering that is similar to that observed in capless

annealing at 500°C. A narrow near-surface region of Cr accumulation in the capped and annealed samples can be attributed to a stress effect induced by the encapsulant. However, the development of a sharply-defined zone of Cr depletion and subsequent gettering within the implanted region can be clearly related to damage nucleation, while the encapsulant stress exerts a relatively minor influence on the mobility of Cr at 500°C. As the annealing temperature is increased, the damage density increases, accompanied by increased motion and gettering of Cr into the implanted region. At 700°C, the encapsulant stress effect becomes more pronounced and increased motion of Cr toward the surface is observed. For annealing temperatures exceeding 700°C, significant damage annihilation occurs and near-surface Cr accumulation and outdiffusion are prevalent. The stress created by the encapsulant at these temperatures is sufficient to move Cr through the residual damage toward the surface, creating a wide depletion zone extending to a depth of $\sim$2 μm into the sample.

15. CONCLUSIONS

In the first phase of this program, we developed a prototype unit for introducing back-surface damage in Si and GaAs wafers and demonstrated that the process can be optimized to produce adequate gettering of defects and impurities in GaAs. It has been shown for the first time that Cr and Au impurities can be gettered by back-surface mechanical damage. Dislocation density gradients and corresponding strain field gradients at the back surface are responsible for the gettering action observed.

Contrasting experiments performed on Ne-implanted GaAs samples have shown mechanical-damage gettering to be superior and more cost effective. In both cases, the annealing cap was shown to exercise a small, but perceptible, influence on gettering of defects at the front surface. Cap gettering was shown to be attributable, in part, to the outdiffusion of Ga and/or As from the substrate, creating localized vacancy-rich regions that aid in defect annihilation. Improvements in cap quality and the elimination of oxygen from nitride encapsulants should aid in reducing apparent cap gettering effects.

Of particular interest for both Si and GaAs gettering is the problem of thermal stability of defects during annealing; the stability period will define the usable time of active gettering during processing cycling or device fabrication. Beyond a fixed period (4 - 5 hours at 800^{o}C for mechanically-induced damage), reverse gettering will occur and impurities will be released from dislocations at the back surface to move into the bulk toward the front surface. For ion-implantation gettering, the problem is an especially acute one, since the induced damage is largely annealed after 1 hour.

To improve the stability time, we used an As-doped SiO_2 cap on the back surface to prevent the loss of As vacancies. It was shown that dislocation structure and ion-induced damage can be retained for longer periods in the presence of an As-doped cap at the interface.

To provide additional information on the gettering behavior of Cr in the presence of dislocation line structures or ion implantation damage, we annealed samples in H_2 at temperatures in the range, 250°C to 500°C and found significant motion of Cr into damage regions, thereby providing the first indication of the low-temperature mobility of Cr in GaAs.

To investigate the applicability of back-surface-damage techniques for improving the quality of epitaxial layers grown on SI-GaAs substrates, VPE layers were prepared (in a standard hydride reactor) on both control (ungettered) and pre-gettered Cr-doped substrates. These experiments showed that Cr motion into the VPE layer was substantially reduced during deposition and subsequent annealing by the gettering treatment.

Investigations of Au contact layers on substrates and LPE layers have shown that Cr is rapidly gettered and outdiffuses during normal alloying at 350°C. It is presently thought that the low-temperature motion of Cr into alloy damage regions and Au thin layers are responsible, in part, for the degradation of Au-Ge-Ni contacts on GaAs after low-temperature thermal aging.

Fabrication of FET device structures in VPE layers grown on pre-gettered substrates, showed considerable improvements compared to devices fabricated on control substrates. It is of particular importance that no pre-screening (selection) tests were used and

the improvements in device yield/wafer were noted, independent of the qualty of the starting substrate material, when pre-getteing processes were used.

Evaluations of GaAs substrates grown by Bridgman and LEC techniques have shown inclusions of B during the growth sequence. It was demonstrated that the boron oxide cap was not a significant factor in introducing B into the lattice, rather, the pBN crucible used in LEC growth was shown to introduce considerable concentrations of B ($\simeq 10^{17}$ cm^{-3}) into the GaAs material. Since many LEC (pBN) substrates contain negligible Cr concentrations, the question of whether B may be contributing directly or indirectly (as a complex) to semi-insulating behavior remains an open conjecture and has not been resolved in these investigations.

To resolve the question of the relative contribution of encapsulant and implantation damage on redistribution of Cr in implanted (front surface) GaAs, we annealed B-implanted samples containing Si_3N_4 caps for 1 hr. at temperatures of 500°C to 900°C in 50°C increments. From the data obtained, we can conclude that the nucleation (or accumulation) of damage can be correlated with the observed Cr depletion and gettering. It is suggested that interactions between Cr atoms and dislocation loops or point defects are responsible for gettering within these damage regions. Annealing of Si_3N_4-capped samples at 500°C produces a pattern of Cr depletion and gettering that is similar to that observed in capless annealing at 500°C. A narrow near-surface region of Cr accumulation in the capped and annealed samples can be attributed to a stress effect induced by the encapsulant. However, the development of a sharply-defined zone of Cr depletion and subsequent gettering within the implanted region can be clearly related to damage nucleation, while the encapsulant stress exerts a relatively minor influence on the mobility of Cr at 500°C. As the annealing temperature is increased, the damage density increases,

accompanied by increased motion and gettering of Cr into the implanted region. At 700°C, the encapsulant stress effect becomes more pronounced and increased motion of Cr toward the surface is observed. For annealing temperatures exceeding 700°C, significant damage annihilation occurs and near-surface Cr accumulation and outdiffusion are prevalent. The stress created by the encapsulant at these temperatures is sufficient to move Cr through the residual damage forward the surface, creating a wide depletion zone extending to a depth $\sim$2 μm into the sample.

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APPENDIX I: TECHNICAL REPORTS PUBLISHED

1. ARACOR Technical Report G-100, "Gettering of Au in GaAs," (May, 1978).

2. ARACOR Technical Report G-101, "Anomalous Diffusion of Cr in GaAs," (July, 1978).

3. ARACOR Technical Report 19-6, "Gettering of Cr in GaAs," (Dec., 1978).

4. C. A. Evans and Assoicates Technical Report D-101, "Trace Level Microanalysis of C and O in Electronic Materials Using Cs Bombardment SIMS," (May, 1980).

5. ARACOR Technical Report 19-1, Interim Report, ONR Contract No. N00014-78-C-0065, (October, 1978).

6. ARACOR Technical Report 19-2, Interim Report, ONR Contract N00014-78-C-0065, (January, 1980).

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Dr. F. Blum/Dr. Daniel Chen 1
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Science Center
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Thousand Oaks, CA 91360

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MSC
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Somerset, NJ 08873

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Hughes Research Laboratory
3011 Malibu Canyon Road
Malibu, CA 90265

Mr. Lothar Wandinger 1
ECOM/AMSEL/TL/IJ
Fort Monmouth, NJ 07003

Dr. Harry Wieder
Naval Ocean Systems Center
Code 922
271 Catalina Blvd.
San Diego, CA 92152 — 1

Dr. William Lindley
MIT
Lincoln Laboratory
F124A, P. O. Box 73
Lexington, MA 02173 — 1

Mr. Sven Roosild
AFCRL/LQD
Hanscom AFB, MA 01731 — 1

Commander
U.S. Army Electronics Command
V. Gelnovatch
(DRSEL-TL-IC)
Fort Monmouth, NJ 07703 — 1

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Cornell University
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Mr. Horst W. A. Gerlach
2800 Powder Mill Road
Adelphia, MD 20783 — 1

Advisory Group on Electron Devices
201 Varick Street, 9th floor
New York, NY 10014 — 1

D. Claxton
MS/1414
TRW Systems
One Space Park
Redondo Beach, CA 90278 — 1

Professor L. Eastman
Phillips Hall
Cornell University
Ithaca, NY 14853 — 1

AIL TECH
612 N. Mary Avenue
Sunnyvale, CA 94086
Attn: D. G. Vendelin — 1

Professors Hauser and Littlejohn
Department of Electrical Engr.
North Carolina State University
Raleigh, NC 27607 — 1

Professor Irving Kaufman
Electrical and Computer Engineering
Arizona State University
Tempe, Arizona 85281 — 1